Document Number: A2T21H140-24S
Rev. 0, 03/2017

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 36 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2110 to 2170 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.5 Vdc, P_{out} = 36 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

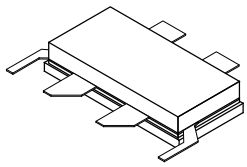
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	17.4	53.1	6.9	–30.2
2140 MHz	17.5	53.3	6.8	–31.4
2170 MHz	17.5	53.0	6.7	–32.1

Features

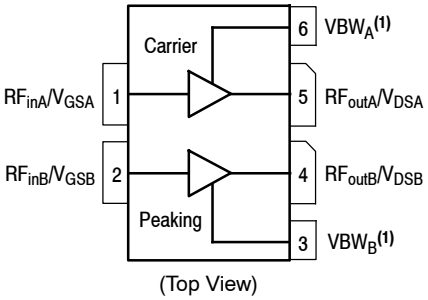
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2T21H140-24SR3

2110–2170 MHz, 36 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-780S-4L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 77°C, 36 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.5 Vdc, 2140 MHz	$R_{\theta JC}$	0.45	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C2

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 70 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 350 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.7 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.5 Vdc, P_{out} = 36 W Avg., f = 2110 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.7	17.4	19.7	dB
Drain Efficiency	η_D	50.1	53.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.4	6.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	–30.2	–26.6	dBc
Load Mismatch (2) (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 350 mA, V_{GSB} = 0.5 Vdc, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 200 W CW Output Power (3 dB Input Overdrive from 120 W CW Rated Power)	No Device Degradation				
Typical Performance (2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 350 mA, V_{GSB} = 0.5 Vdc, 2110–2170 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (3)	P3dB	—	169	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	–23	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 36 W Avg.	G_F	—	0.18	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.008	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T21H140-24SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

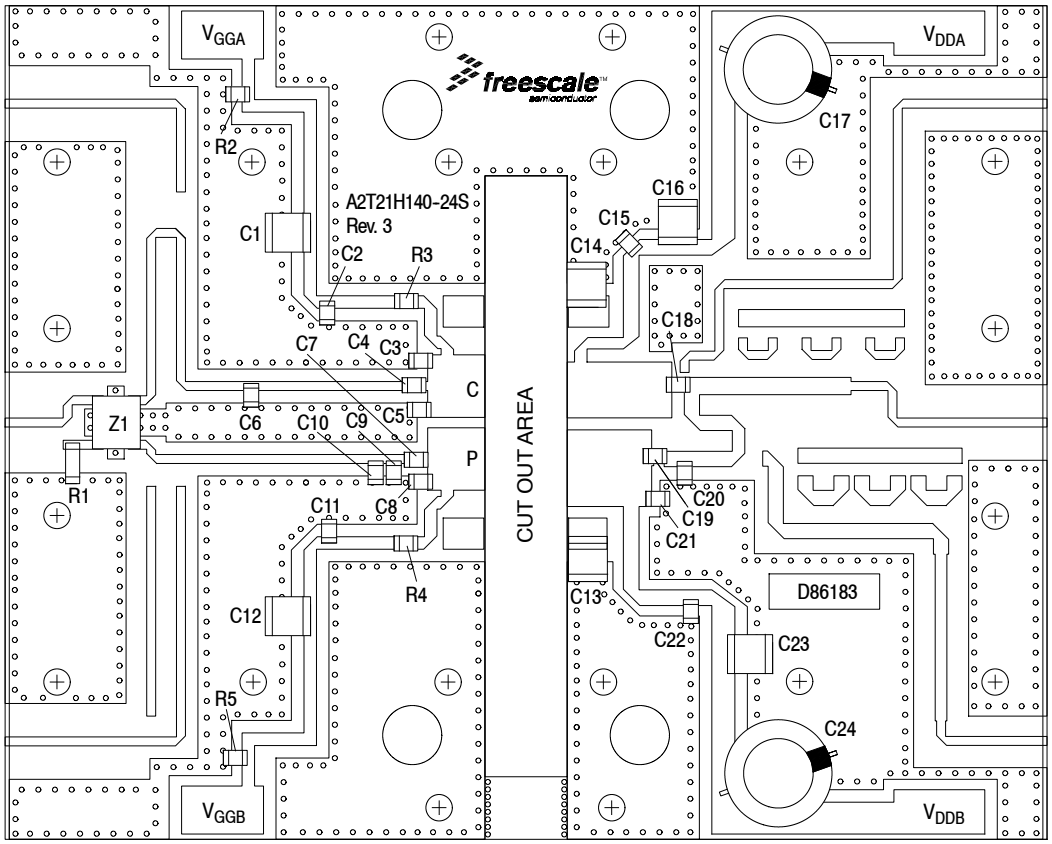


Figure 2. A2T21H140-24SR3 Test Circuit Component Layout

Table 6. A2T21H140-24SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C12, C13, C14, C16, C23	10 μF Chip Capacitor	C5750X7S2A106M	TDK
C2, C4, C7, C11, C15, C19, C22	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C3	1.6 pF Chip Capacitor	ATC600F1R6BT250XT	ATC
C5, C10, C20	0.3 pF Chip Capacitor	ATC600F0R3BT250XT	ATC
C6	0.1 pF Chip Capacitor	ATC600F0R1BT250XT	ATC
C8	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C9	0.2 pF Chip Capacitor	ATC600F0R2BT250XT	ATC
C17, C24	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C18	9.1 pF Chip Capacitor	ATC600F9R1BT250XT	ATC
C21	0.4 pF Chip Capacitor	ATC600F0R4BT250XT	ATC
R1	50 Ω, 4 W Chip Resistor	C10A50Z4	Anaren
R2, R5	20 kΩ, 1/4 W Chip Resistor	CRCW120620K0JNEA	Vishay
R3, R4	5.1 Ω, 1/4 W Chip Resistor	CRCW12065R10FKEA	Vishay
Z1	2000–2300 MHz Band, 90°, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D86183	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHz

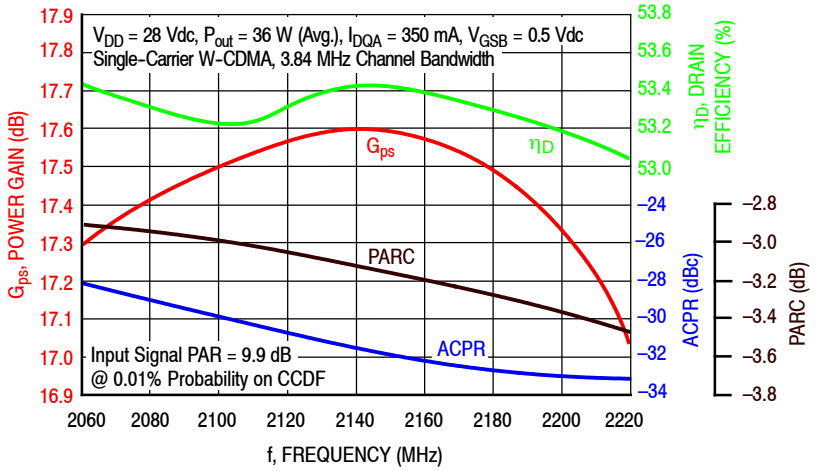


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 36 Watts Avg.

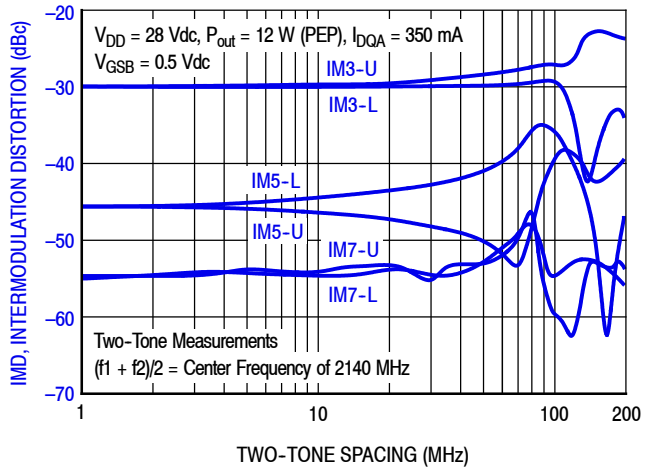


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

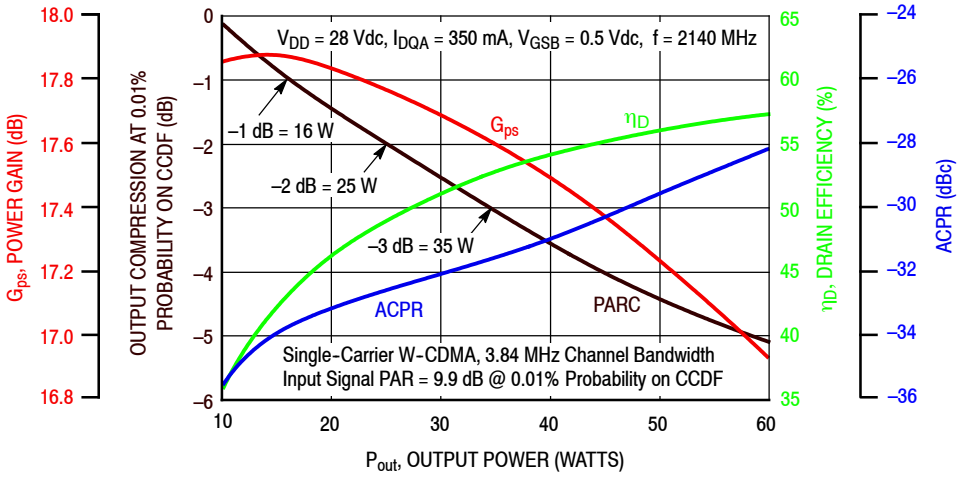


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

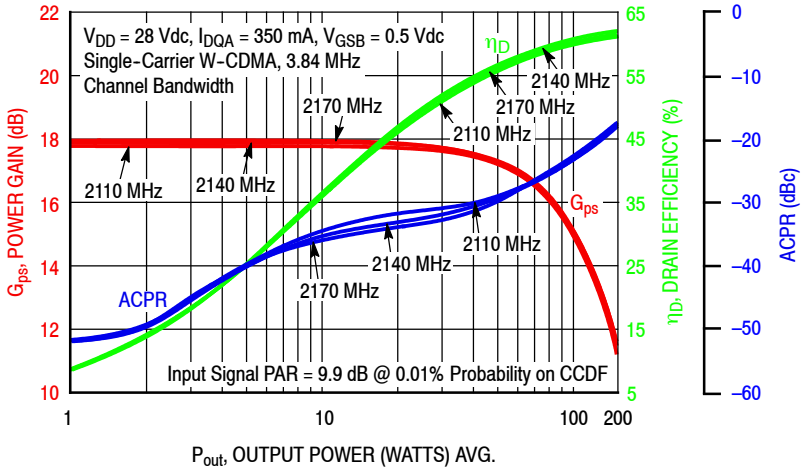


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

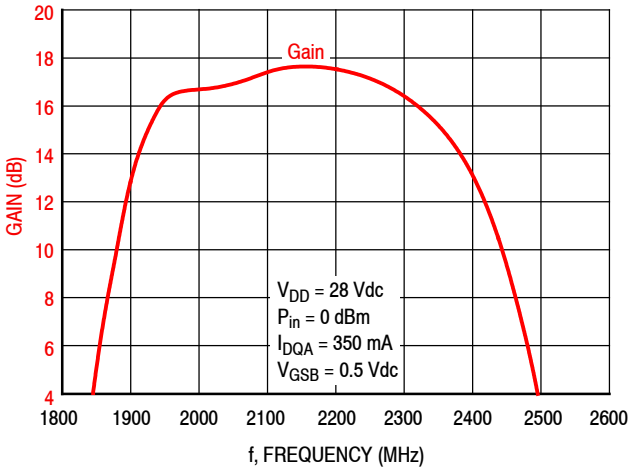


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 355 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	11.6 – j15.5	10.4 + j14.9	5.77 – j12.5	19.2	48.8	76	53.7	–16
2140	15.8 – j15.3	13.7 + j15.3	5.77 – j10.6	19.3	48.8	76	55.6	–17
2170	19.4 – j11.9	17.8 + j13.4	5.88 – j11.2	19.2	48.8	77	55.6	–16

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	11.6 – j15.5	11.9 + j16.0	5.74 – j12.6	17.2	49.6	91	55.6	–21
2140	15.8 – j15.3	16.2 + j15.8	5.91 – j12.0	17.1	49.6	91	56.5	–22
2170	19.4 – j11.9	21.0 + j12.6	6.02 – j12.4	17.0	49.6	92	56.5	–21

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

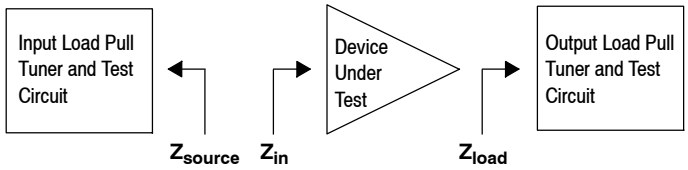
Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQA} = 355 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	11.6 – j15.5	9.85 + j17.0	11.9 – j3.16	22.8	46.2	42	66.1	–28
2140	15.8 – j15.3	13.9 + j17.0	9.84 – j5.25	21.9	47.1	52	66.4	–25
2170	19.4 – j11.9	18.9 + j15.3	9.56 – j4.82	22.0	47.0	50	66.7	–26

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	11.6 – j15.5	11.2 + j17.5	10.5 – j5.83	20.1	47.8	60	66.2	–33
2140	15.8 – j15.3	15.8 + j18.3	8.46 – j5.24	19.7	47.9	62	67.1	–36
2170	19.4 – j11.9	22.0 + j15.6	8.08 – j5.38	19.6	47.9	62	67.4	–35

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

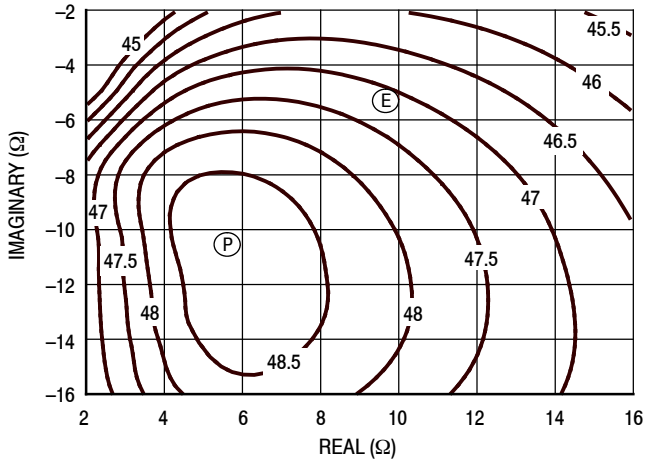


Figure 8. P1dB Load Pull Output Power Contours (dBm)

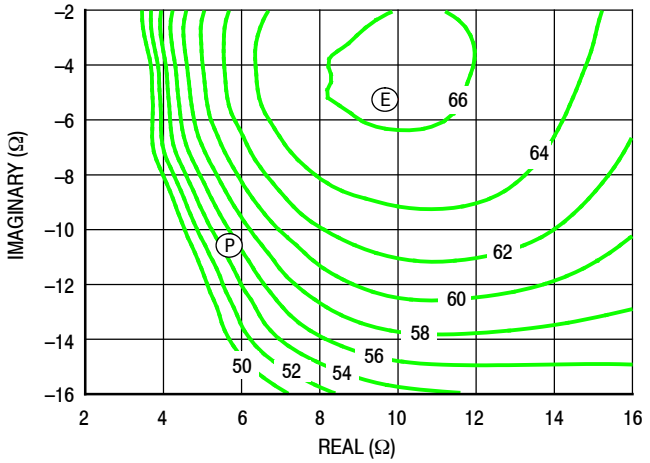


Figure 9. P1dB Load Pull Efficiency Contours (%)

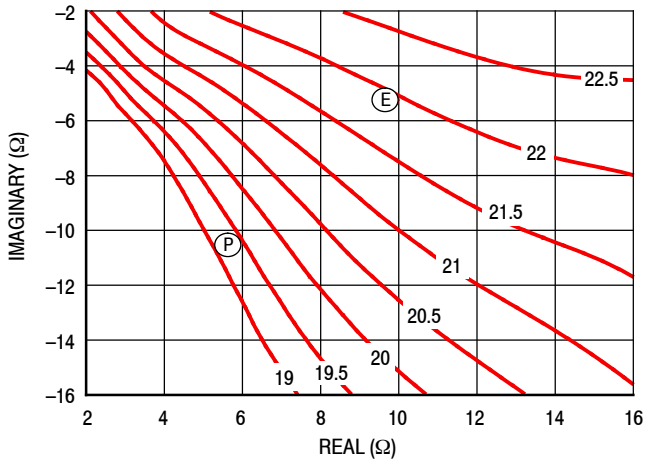


Figure 10. P1dB Load Pull Gain Contours (dB)

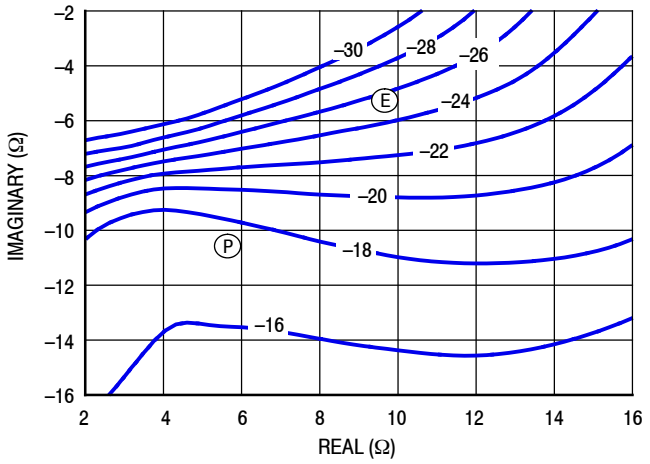


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2140 MHz

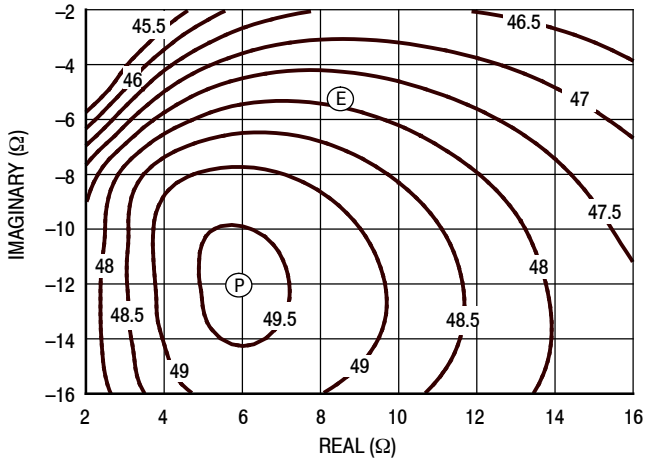


Figure 12. P3dB Load Pull Output Power Contours (dBm)

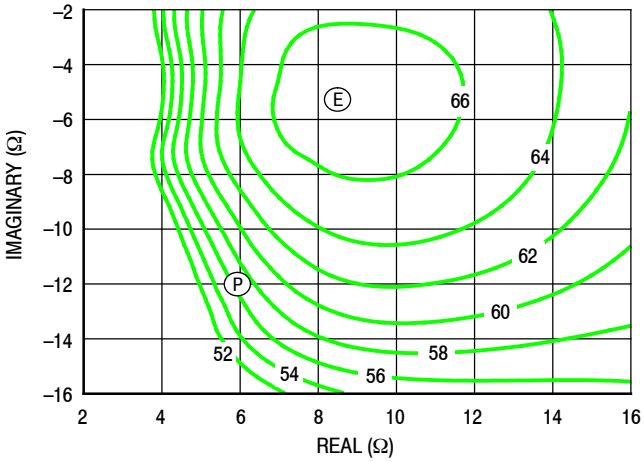


Figure 13. P3dB Load Pull Efficiency Contours (%)

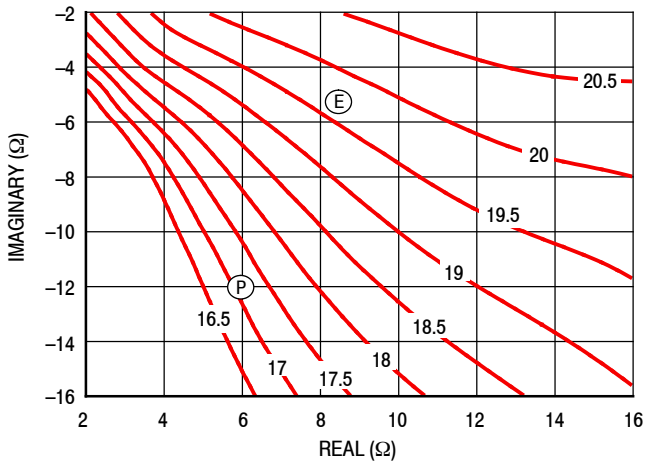


Figure 14. P3dB Load Pull Gain Contours (dB)

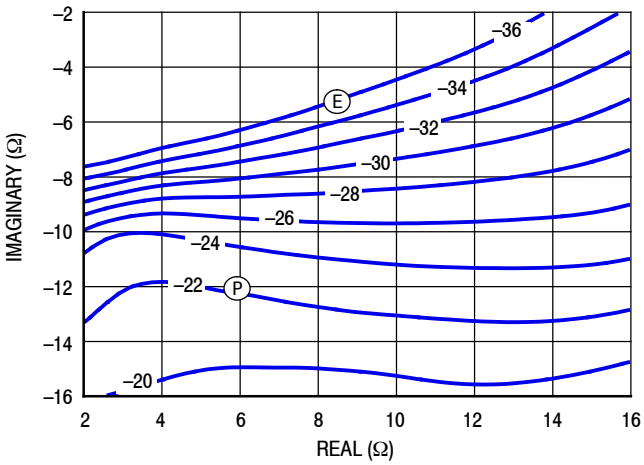


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	10.2 – j17.7	11.6 + j18.7	5.96 – j12.8	14.5	50.5	113	56.5	–29
2140	13.9 – j18.3	16.0 + j19.0	6.26 – j13.0	14.5	50.5	112	56.8	–30
2170	19.5 – j16.1	21.7 + j17.2	6.42 – j13.3	14.4	50.5	113	57.2	–30

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	10.2 – j17.7	13.8 + j19.4	6.34 – j13.6	12.4	51.3	134	58.1	–36
2140	13.9 – j18.3	19.3 + j18.8	6.62 – j13.9	12.4	51.2	132	57.6	–37
2170	19.5 – j16.1	25.4 + j14.9	6.85 – j14.3	12.3	51.2	132	57.8	–37

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

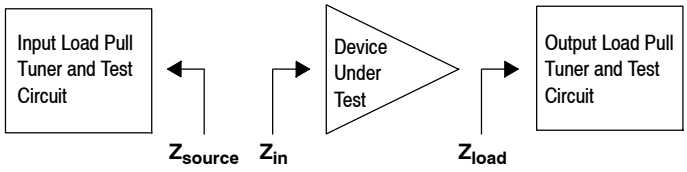
Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	10.2 – j17.7	9.39 + j20.4	11.1 – j5.75	16.0	48.6	73	70.2	–34
2140	13.9 – j18.3	13.5 + j22.1	10.3 – j4.94	15.9	48.4	68	70.0	–36
2170	19.5 – j16.1	20.4 + j21.8	9.59 – j6.35	15.7	48.8	75	70.0	–36

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	10.2 – j17.7	12.2 + j21.0	11.6 – j8.27	13.9	49.8	95	69.7	–42
2140	13.9 – j18.3	17.9 + j21.8	11.2 – j7.51	13.8	49.6	91	69.3	–44
2170	19.5 – j16.1	25.6 + j19.4	10.4 – j7.20	13.7	49.5	89	69.4	–45

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

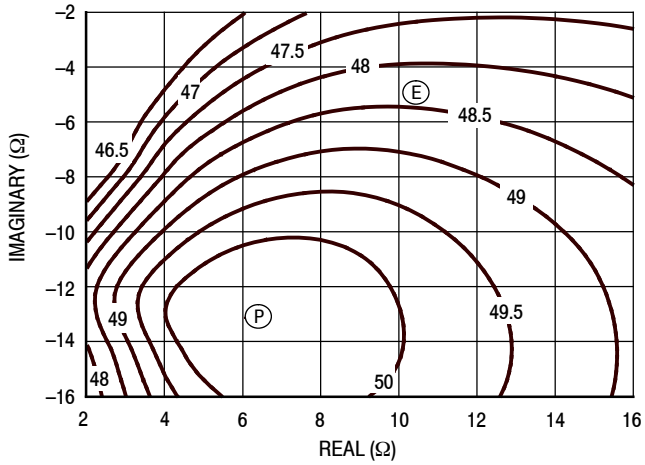


Figure 16. P1dB Load Pull Output Power Contours (dBm)

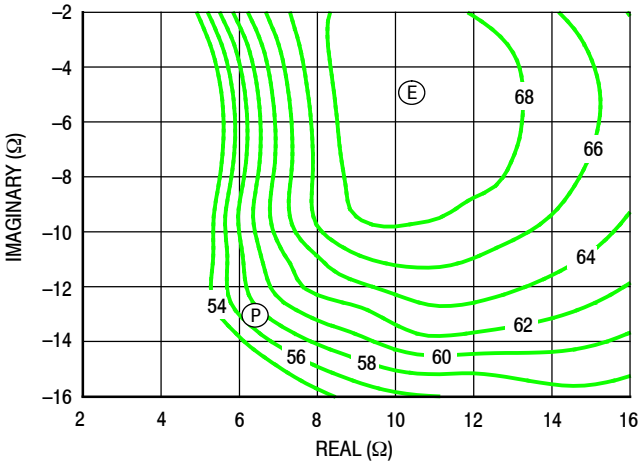


Figure 17. P1dB Load Pull Efficiency Contours (%)

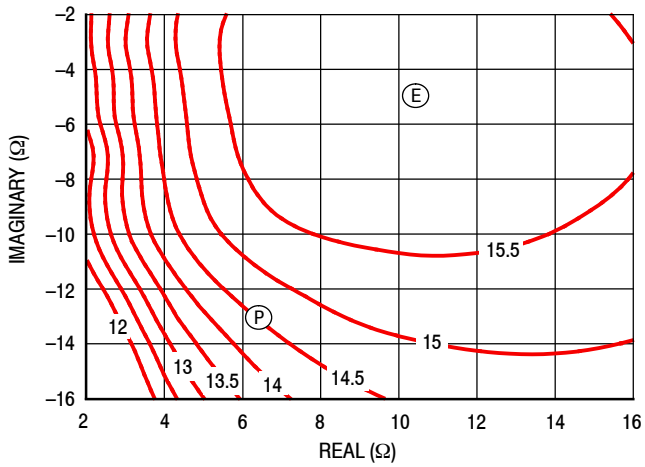


Figure 18. P1dB Load Pull Gain Contours (dB)

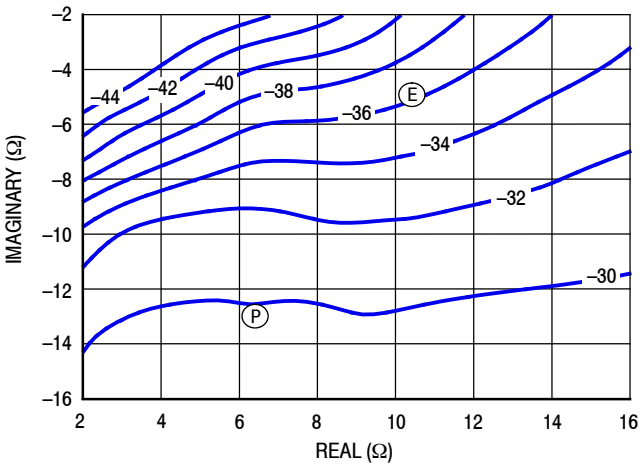


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2140 MHz

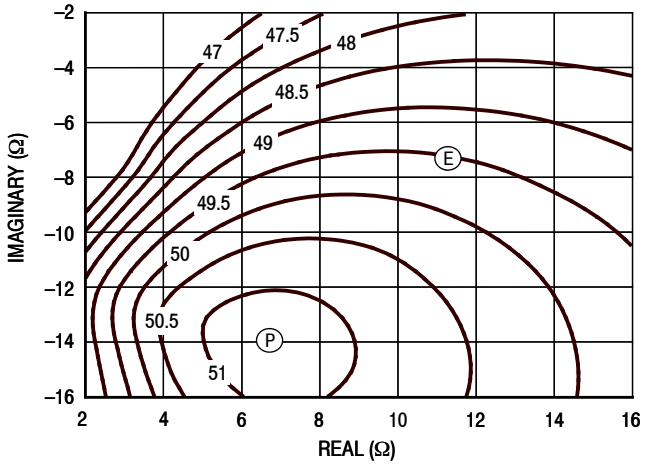


Figure 20. P3dB Load Pull Output Power Contours (dBm)

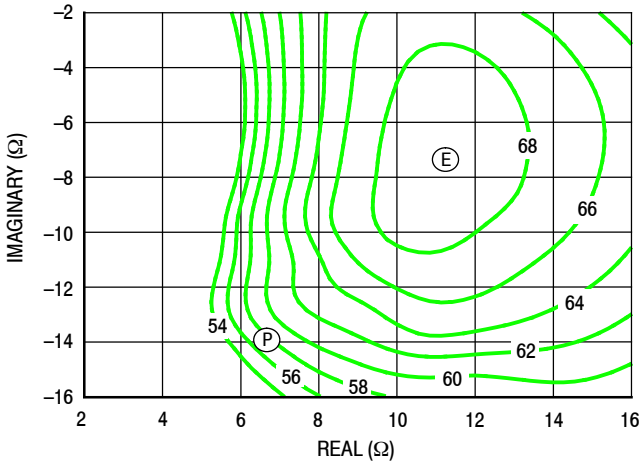


Figure 21. P3dB Load Pull Efficiency Contours (%)

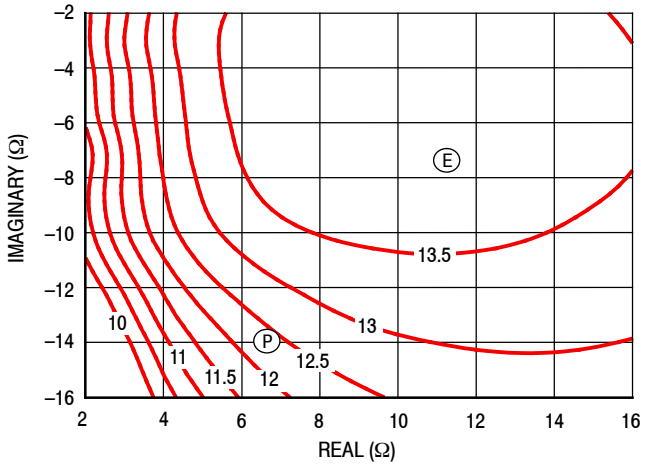


Figure 22. P3dB Load Pull Gain Contours (dB)

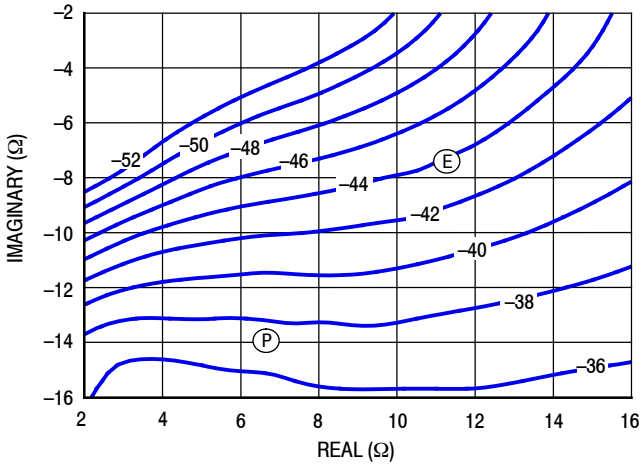


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

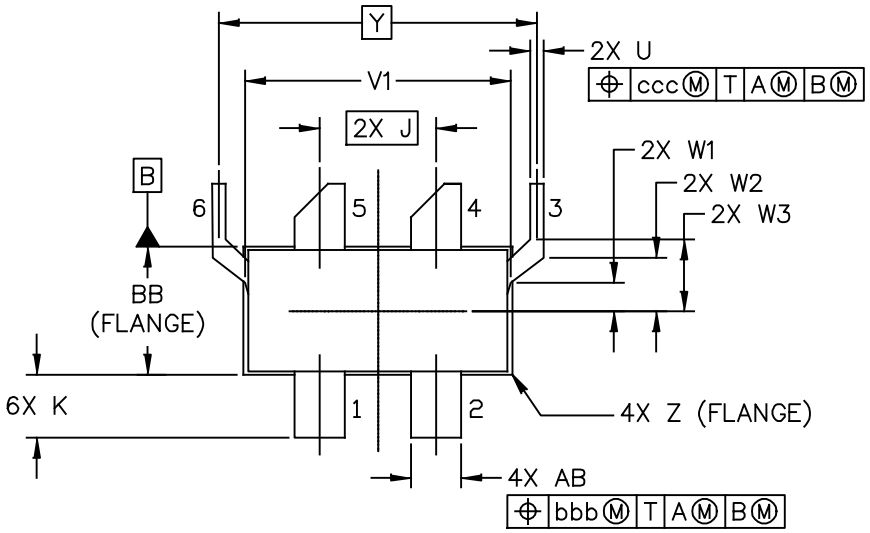
Gain

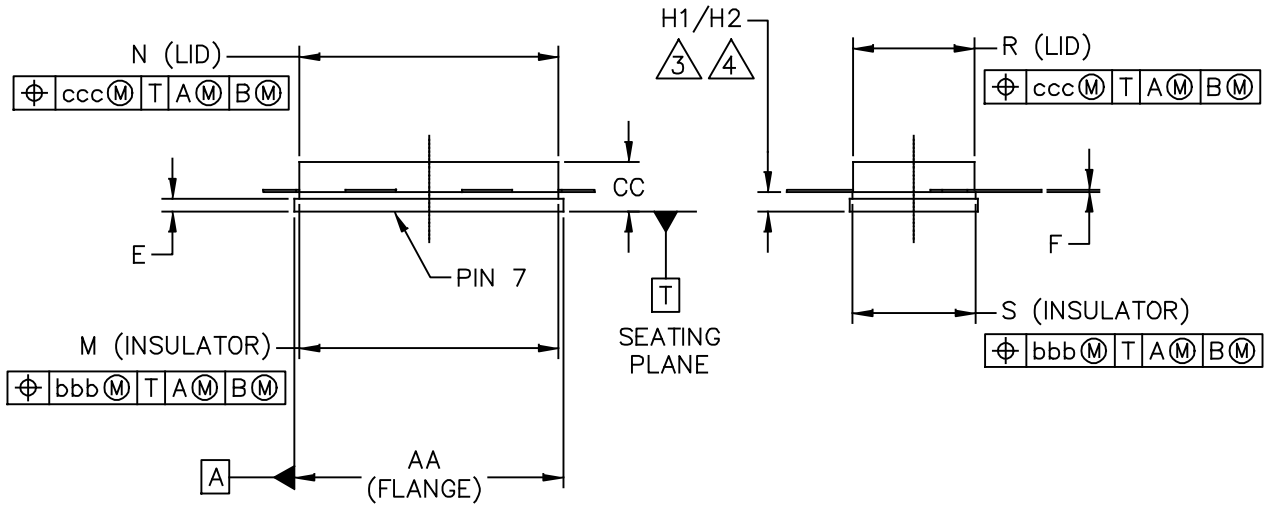
Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS





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	SOT1799−3	18 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.
4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
E	.035	.045	0.89	1.14	V1	.795	.805	20.19	20.45
F	.004	.007	0.10	0.18	W1	.080	.090	2.03	2.29
H1	.057	.067	1.45	1.70	W2	.155	.165	3.94	4.19
H2	.054	.070	1.37	1.78	W3	.210	.220	5.33	5.59
J	.350 BSC		8.89 BSC		Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	AB	.145	.155	3.68	3.94
N	.772	.788	19.61	20.02	aaa	.005		0.13	
					bbb	.010		0.25	
					ccc	.015		0.38	

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SOT1799–3 18 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2017	• Initial release of data sheet

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