CEL California Eastern Laboratories

Evaluation Board Document

µPG2415T6X-EVAL-A

Evaluation Board

- Description
- Insertion Loss of Through Board
- Assembly Drawing

Description:

The uPG2415T6X-EVAL-A evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2415T6X switch. In addition to the device, the board provides DC block capacitors, power supply bypass capacitors, and RF and DC connectors.

A DC block capacitor is required at all RF ports. On this board, two parallel capacitors of 22pF are used for this purpose. This configuration minimizes the mismatch effect associated with the serial capacitors over a wide frequency range. In a real application where the operation frequency range is relatively narrow, one DC block capacitor usually is sufficient. The user should select the appropriate capacitor value according to the operation frequencies and the type of capacitor selected. Generally the performance of the switch circuit is not sensitive, to a certain extent, to the value of DC block capacitors.

A 1000pF DC bypass capacitor is used on all control lines. For high speed applications the user may choose smaller capacitance.

Board Material:

The board material is 20 mil thick Duroid 6002. Its dielectric constant is 2.94.

Switch Logic Table:

The following table lists the logic table for switch states.

Vcont1	Vcont2	RFC – RF1	RFC – RF2
H	L	ON	OFF
L	H	OFF	ON

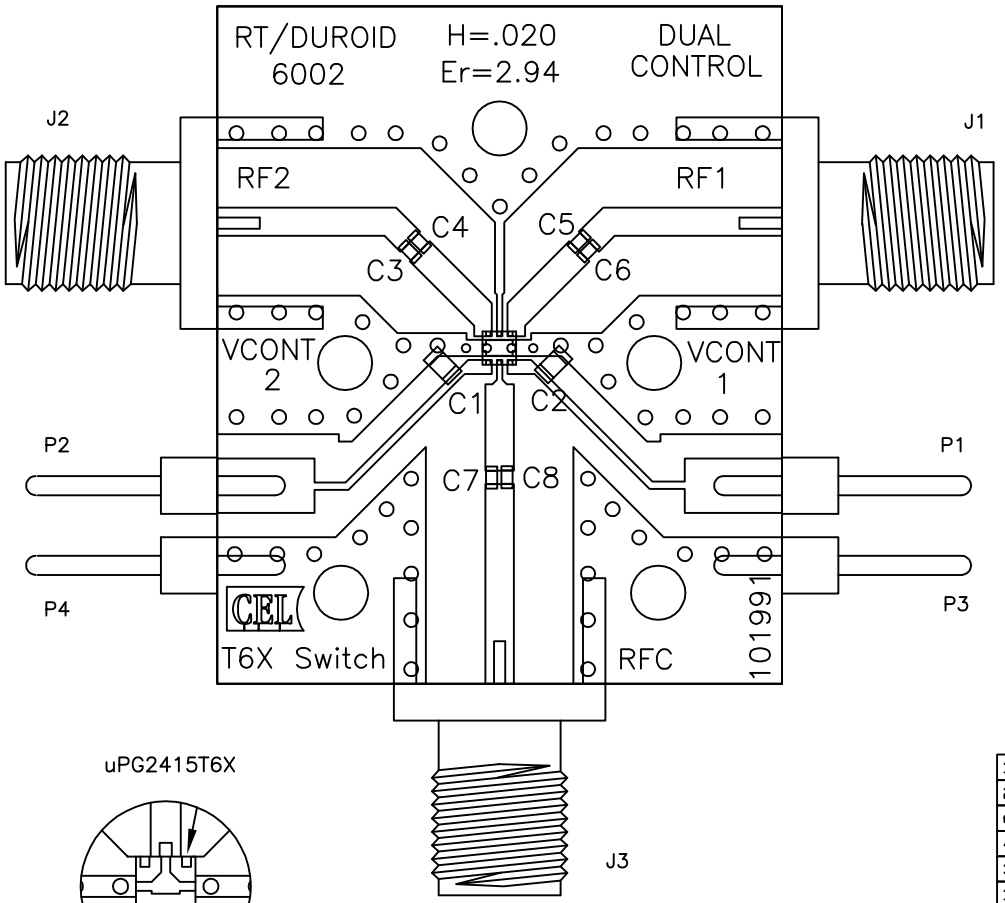
Insertion Loss of Through Board:

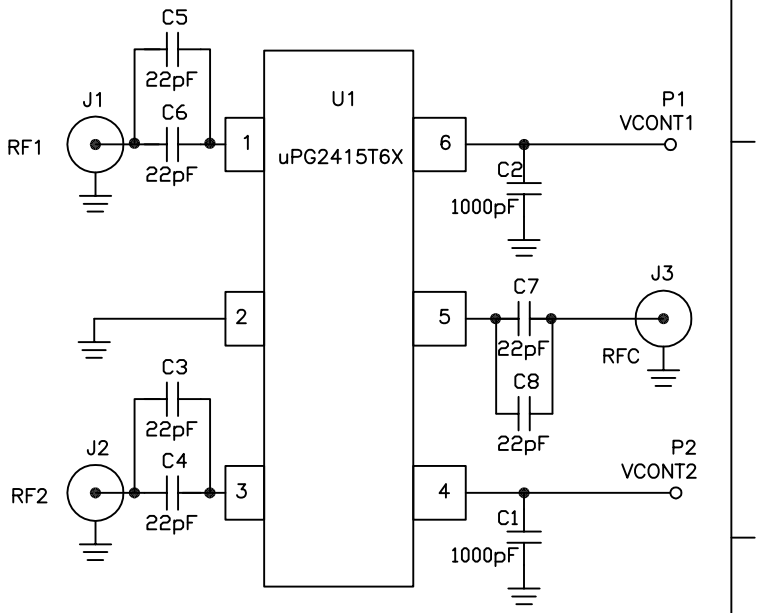
The measured insertion loss (S21) of the board is from three contributions: the switch insertion loss, the loss in the DC block capacitors and the insertion loss of the through board. To accurately estimate the insertion loss due to the switch circuit, the board loss should be subtracted from the measured S21 value. The table below lists the board loss at different frequencies. The effect of the capacitor loss is not corrected since in real applications DC block capacitors are required. Nevertheless the capacitor loss can be significant, particularly at high frequencies. For applications where insertion loss is critically important, the DC block capacitor should be carefully chosen to minimize its loss at operation frequency.

INPUT FREQUENCY (GHz)	BOARD LOSS (dB)
0.5	0.05
1.0	0.07
2.0	0.12
2.5	0.13
3.8	0.18
5.0	0.23
6.0	0.29

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Note: C1 and C2 should be placed close to device





uPG2415T6X

MARKING FOR PIN1
IS ON TOP OF CHIP

PACKAGE MARKING: G6E

QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	TF-101481	DRAWING	TEST BLOCK	7
2	GRM1885C1H102JA01D	C1,C2	0603 1000pF CAP MURATA	6
6	GRM1555C1H220JZ01D	C3,C4,C5,C6,C7,C8	0402 22pF CAP MURATA	5
4	2340-6111 TG	P1,P2,P3,P4	PIN HEADER 3M	4
3	5308-2CC	J1,J2,J3	SMA FEMALE CONNECTOR TENSOLITE	3
1	uPG2415T6X	U1	IC NEC uPG2415T6X GaAs Switch	2
1	CL-101991	DRAWING	COMPONENT LAYOUT DRAWING	1

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING

MATERIAL

FINISH

APPROVALS		
Drawing by:	M Dong	02/15/2010
Designed by:	M Dong	02/15/2010
Checked by:		
Project Engineer:		
Quality Control:		

CEL CALIFORNIA EASTERN LABS
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TITLE:
ASSEMBLY DRAWING
uPG2415T6X-EVAL-A

SIZE	FSCM NO.	DWG NO.	REV
C		AD-102005	-

SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 1 OF 1