2.7V to 5.5V, 1.2A 1ch Synchronous Buck Converter with Integrated FET

BD9123MUV

General Description

BD9123MUV is ROHM's high efficiency step-down switching regulator designed to produce voltage as low as 0.85V to 1.2V from a supply voltage of 5V/3.3V. It offers high efficiency by using pulse skip control technology and synchronous switches, and provides fast transient response to sudden load changes by implementing current mode control.

Features

- Fast Transient Response with Current Mode PWM Control System.
- High Efficiency for All Load Range with Synchronous Rectifier (Nch/Pch FET) and SLLM™ (Simple Light Load Mode)
- Output Voltage Selector (3 bit)
- PGOOD Function
- Soft-Start Function
- Thermal Shutdown and UVLO Functions.
- Short-Circuit Protection Circuit with Time Delay Function.
- Shutdown Function

Applications

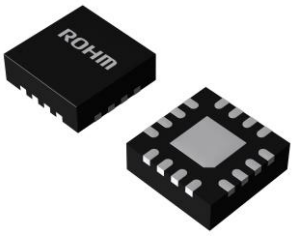
Power Supply for LSI including DSP, Microcomputer and ASIC

Key Specifications

- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range: 0.85V to 1.2V
- Output Current: 1.2A (Max)
- Switching Frequency: 1MHz(Typ)
- Pch FET ON-Resistance: 0.35Ω(Typ)
- Nch FET ON-Resistance: 0.25Ω(Typ)
- Standby Current: 0μA (Typ)
- Operating Temperature Range: -40°C to +95°C

Package

W(Typ) x D(Typ) x H(Max)



VQFN016V3030
3.00mm x 3.00mm x 1.00mm

Typical Application Circuit

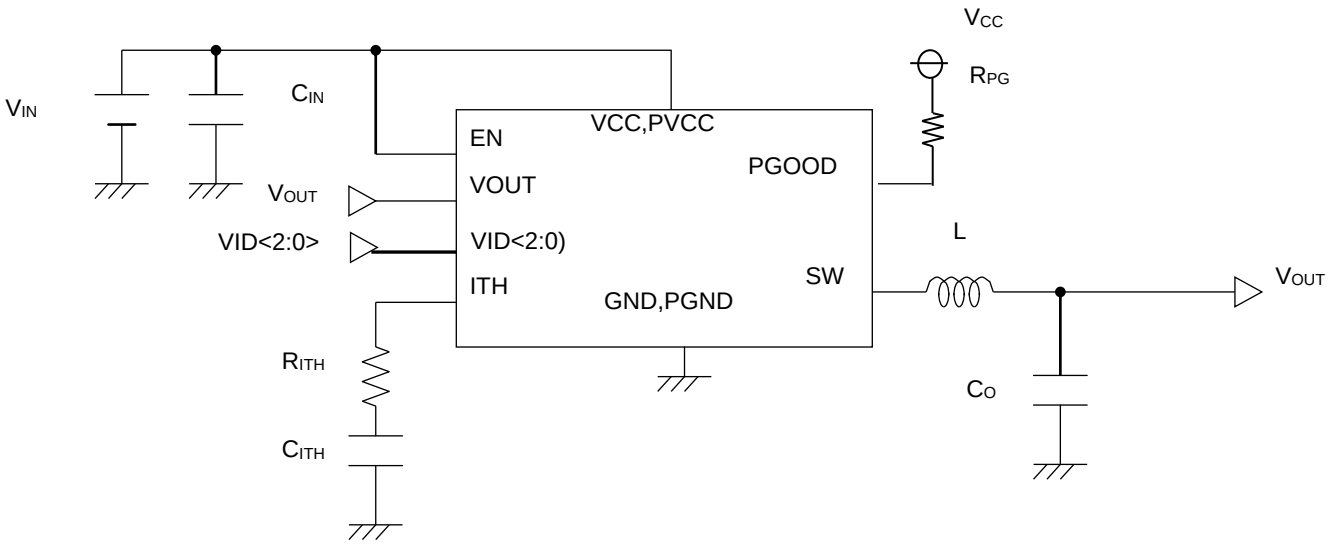


Figure 1. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○ This product has no designed protection against radioactive rays

Pin Configuration

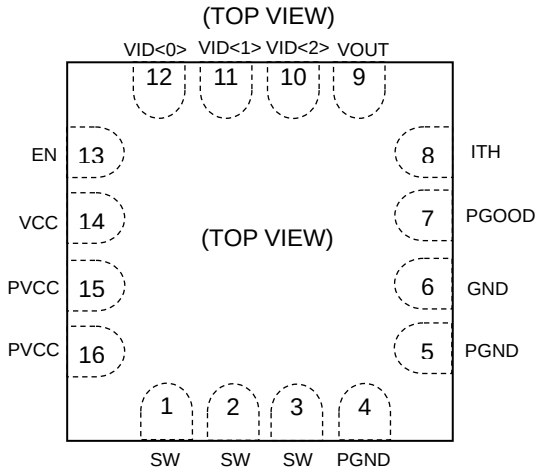


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin name	Function
1	SW	Pch/Nch FET drain output pin
2		
3		
4	PGND	Nch FET source pin
5		
6	GND	Ground
7	PGOOD	Power good pin
8	ITH	Gm Amp output pin/connected phase compensation capacitor
9	VOUT	Output voltage pin
10	VID<2>	Output voltage control pin<2>
11	VID<1>	Output voltage control pin<1>
12	VID<0>	Output voltage control pin<0>
13	EN	Enable pin(High Active）
14	VCC	VCC power supply input pin
15	PVCC	Pch FET source pin
16		

Block Diagram

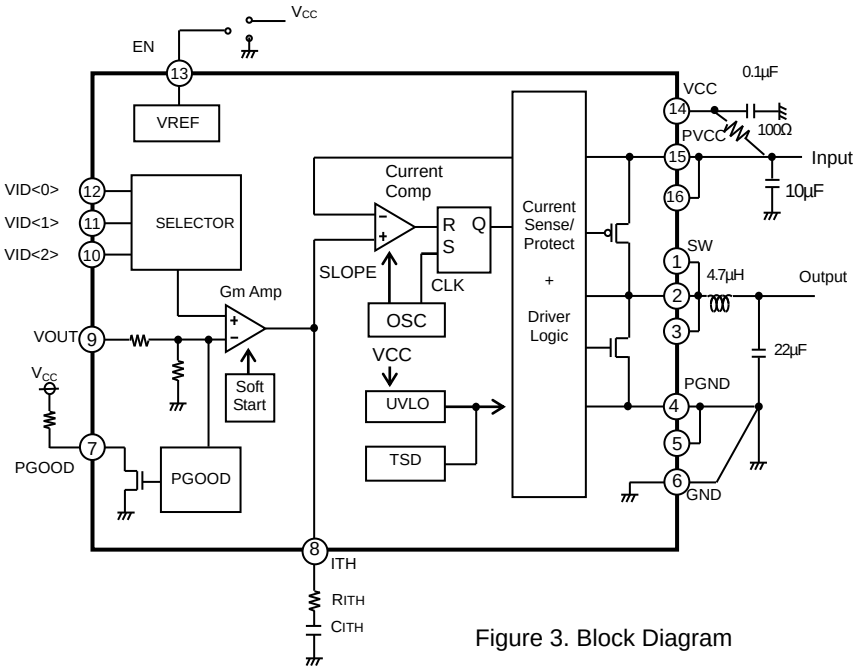


Figure 3. Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
VCC Voltage	V_{CC}	-0.3 to +7 (Note 1)	V
PVCC Voltage	PV_{CC}	-0.3 to +7 (Note 1)	V
EN,SW,ITH Voltage	V_{EN}, V_{SW}, V_{ITH}	-0.3 to +7	V
Logic Input Voltage	$V_{VID<2:0>}$	-0.3 to +7	V
Power Dissipation 1	Pd1	0.27 (Note 2)	W
Power Dissipation 2	Pd2	0.62 (Note 3)	W
Power Dissipation 3	Pd3	1.77 (Note 4)	W
Power Dissipation 4	Pd4	2.66 (Note 5)	W
Operating Temperature Range	Topr	-40 to +95	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Pd should not be exceeded.
(Note 2) IC only
(Note 3) Mounted on a 1-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, occupied area by copper foil : 6.28mm^2
(Note 4) Mounted on a 4-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, 1st and 4th copper foil area : 6.28mm^2 , 2nd and 3rd copper foil area : 5505mm^2
(Note 5) Mounted on a 4-layer 74.2mmx74.2mmx1.6mm glass-epoxy board, occupied area by copper foil : 5505mm^2, in each layers
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +95°C)

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	2.7	3.3	5.5	V
	PV_{CC}	2.7	3.3	5.5	V
EN Voltage	V_{EN}	0	-	V_{CC}	V
Logic Input Voltage	$V_{VID<2:0>}$	0	-	5.5	V
Output Voltage Setting Range	V_{OUT}	0.85	-	1.2	V
SW Average Output Current	I_{SW}	-	-	1.2(Note 6)	A

(Note 6) Pd should not be exceeded.

Electrical Characteristics

(Ta=25°C V_{CC}=PV_{CC}=5V, V_{EN}=V_{CC}, $V_{VID<2>}$= $V_{VID<1>}$= $V_{VID<0>}$= 0V, unless otherwise specified.)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Active Current	I_{CC}	-	300	500	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active mode
EN Input Current	I_{EN}	-	5	10	μA	V_{EN}=5V
VID Low Voltage	V_{VIDL}	-	GND	0.8	V	
VID High Voltage	V_{VIDH}	2.0	V_{CC}	-	V	
VID Input Current	I_{VID}	-	5	10	μA	V_{VID}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
Output Voltage	V_{OUT}	0.98	1.0	1.02	V	$V_{VID<2:0>}$=(0,0,0)
ITH Sink Current	I_{THSI}	25	50	-	μA	V_{OUT} =1.2V
ITH Source Current	I_{THSO}	25	50	-	μA	V_{OUT} =0.8V
UVLO Threshold Voltage	V_{UVLO1}	2.4	2.5	2.6	V	V_{CC}=5V to 0V
UVLO Release Voltage	V_{UVLO2}	2.425	2.55	2.7	V	V_{CC}=0V to 5V
Power Good Threshold	V_{PGOOD1}	70	75	80	%	V_{OUT} to 0V
Power Good Release	V_{PGOOD2}	85	90	95	%	0V to V_{OUT}
Power Good Delay	t_{PG}	2.5	5	10	ms	
PGOOD ON-Resistance	R_{ONPG}	-	140	280	Ω	
Soft-Start Time	t_{SS}	0.4	0.8	1.6	ms	
Timer Latch Time	t_{LATCH}	1	2	4	ms	
Output Short Circuit Threshold Voltage	V_{SCP}	-	V_{OUT}x0.5	V_{OUT}x0.7	V	V_{OUT} to 0V

Typical Performance Curves

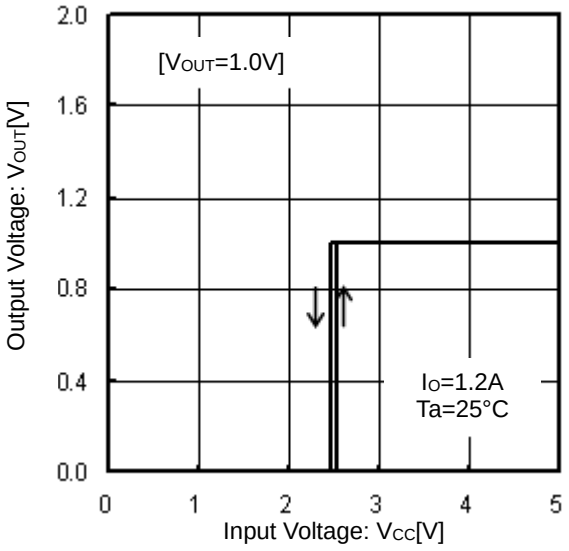


Figure 4. Output Voltage vs Input Voltage

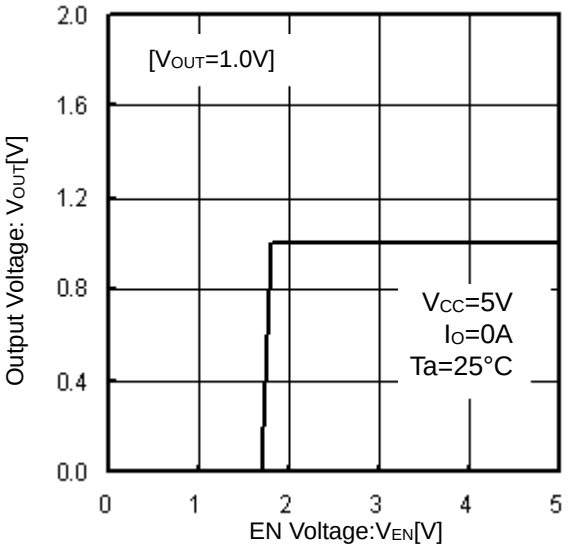


Figure 5. Output Voltage vs EN Voltage

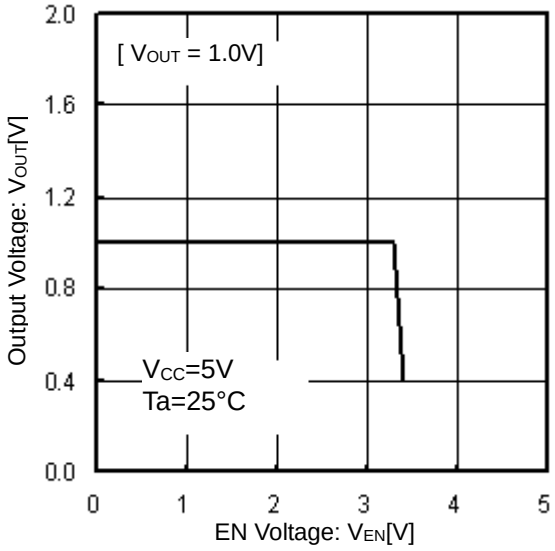


Figure 6. Output Voltage vs EN Volatge

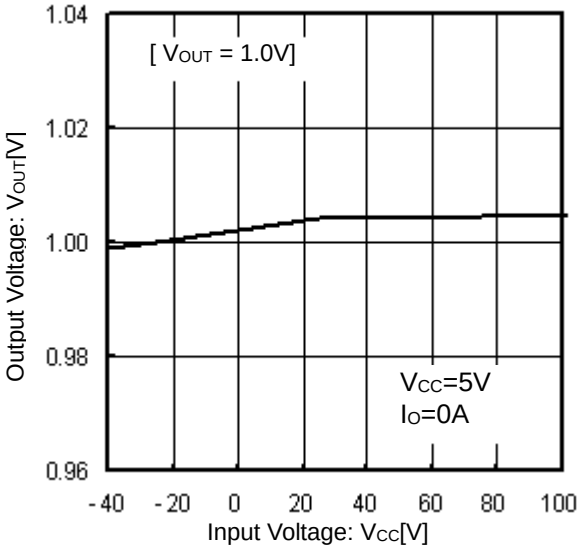


Figure 7. Output Voltage vs Input Voltage

Typical Performance Curves - continued

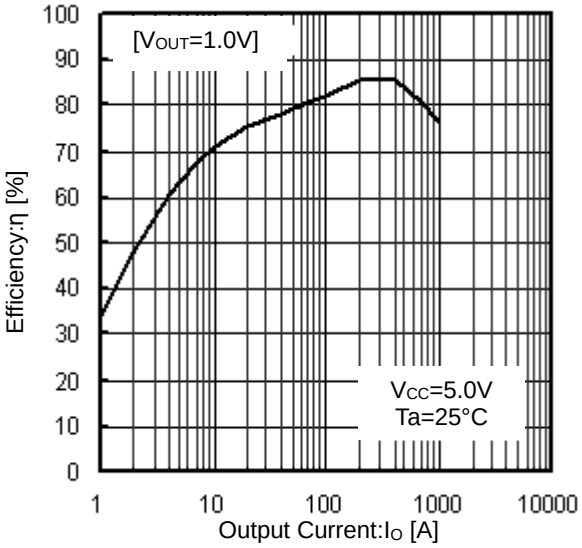


Figure 8. Efficiency vs Output

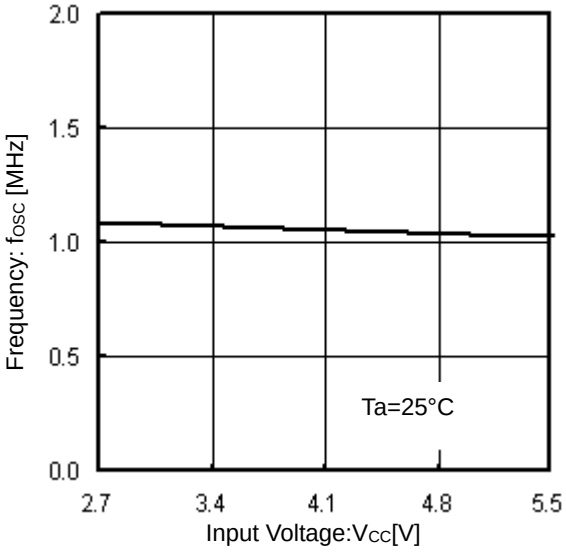


Figure 9. Frequency vs Input Voltage

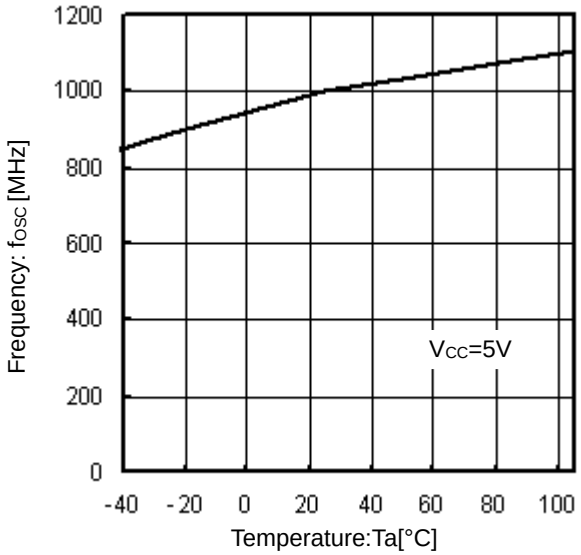


Figure 10. Frequency vs Temperature

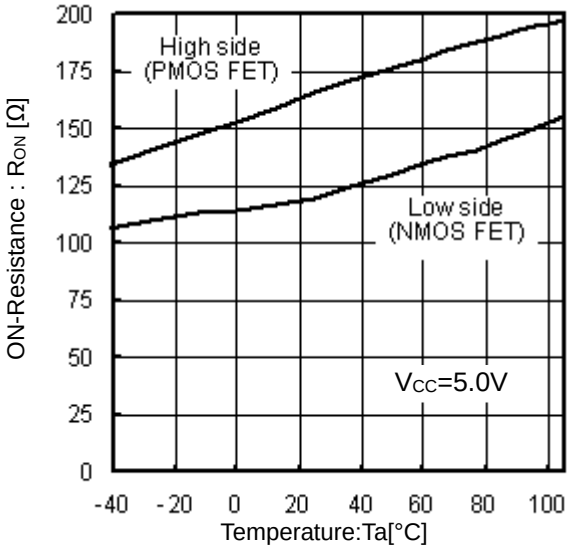


Figure 11. On-Resistance vs Temperature

Typical Performance Curves - continued

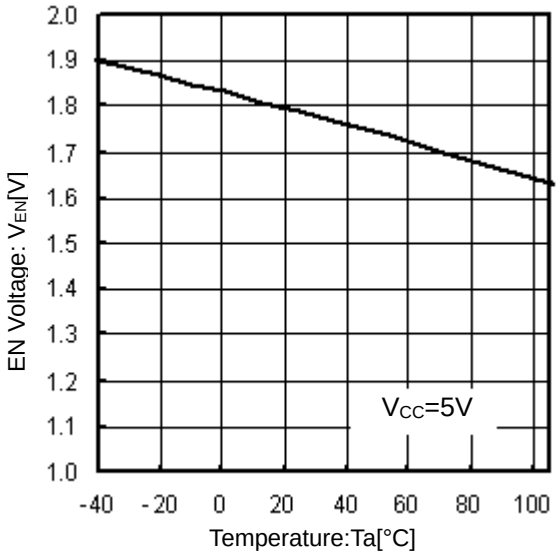


Figure 12. EN Voltage vs Temperature

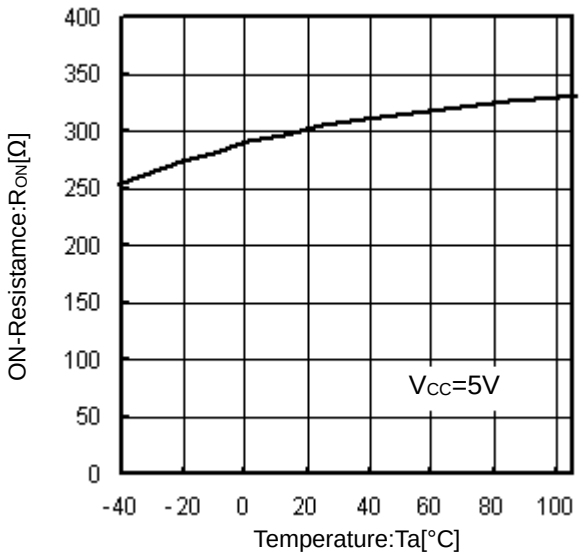


Figure 13. ON-Resistance vs Temperature

Typical Waveforms

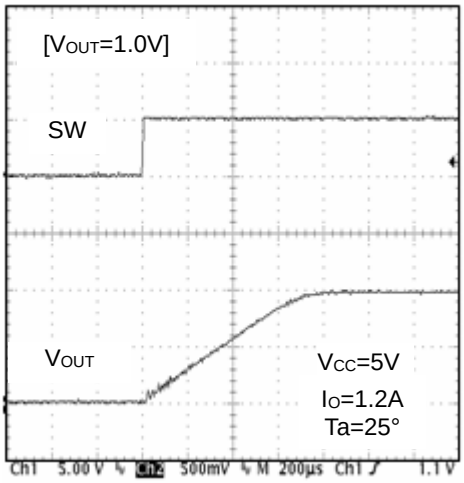


Figure 14. Soft-Start Waveform

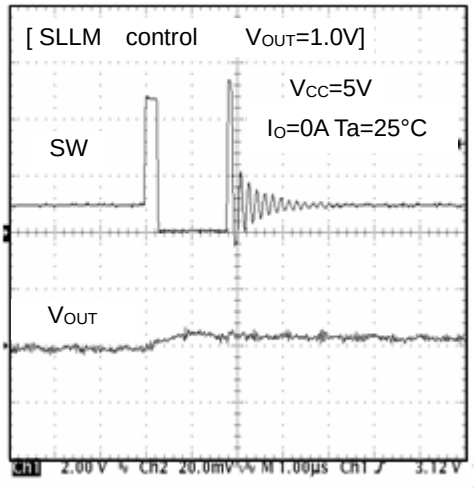


Figure 15. SW Waveform
(I_O=0mA)

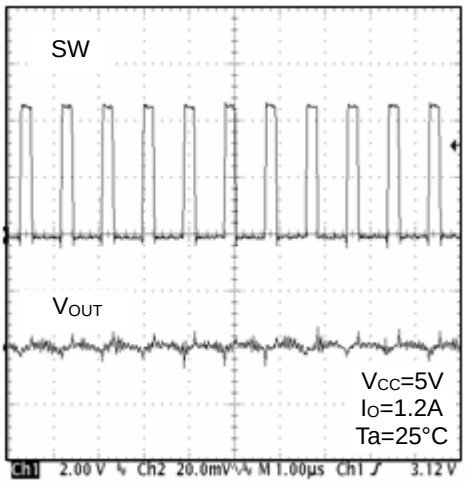


Figure 16. SW Waveform
(I_O=1.2A)

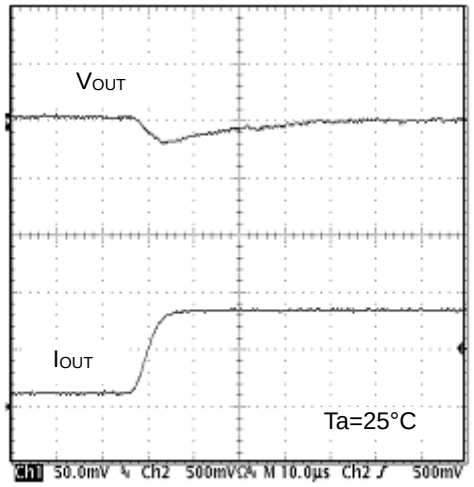


Figure 17. Transient Response
(I_O=125mA to 850mA, 2µA)

Typical Waveforms – continued

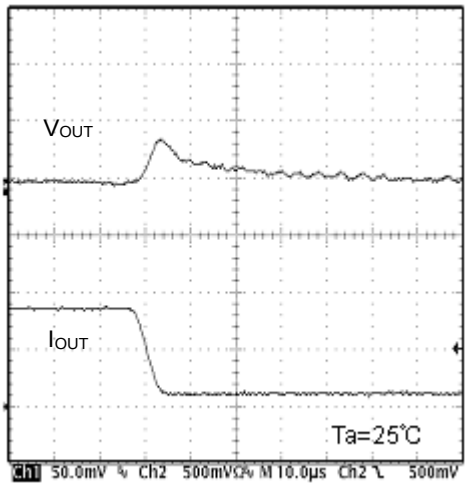


Figure 18. Transient Response
(I_O=850mA～125mA, 2µA)

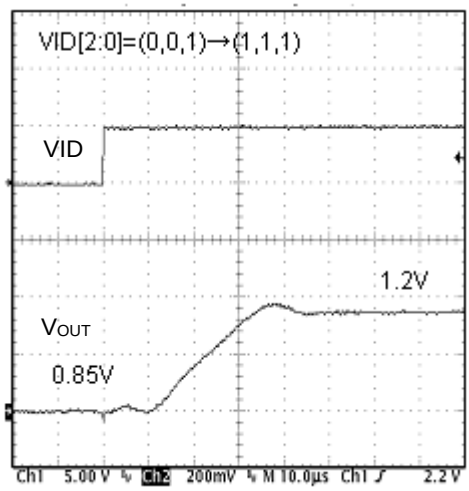


Figure 19. Bit Chance Response

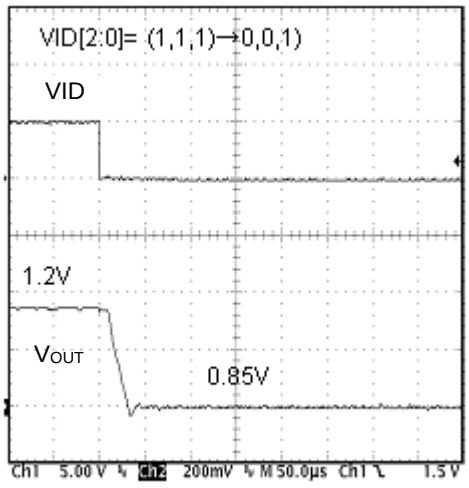


Figure 20. Bit Chance Response

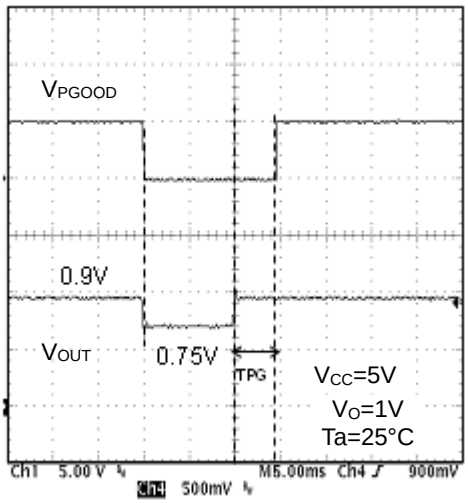


Figure 21. PGOOD Delay

Application Information

1. Operation

BD9123MUV is a synchronous rectifying step-down switching regulator that achieves faster transient response by employing current mode PWM control system. Its switching operation utilizes PWM (Pulse Width Modulation) mode for heavier load, while SLLM™ (Simple Light Load Mode) operation for lighter load to improve efficiency.

(1) Synchronous Rectifier

Integrated synchronous rectification using two MOSFETS reduces power dissipation and increases efficiency when compared to converters using external diodes. Internal shoot-through current limiting circuit further reduces power dissipation.

(2) Current Mode PWM Control

The PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

(a) PWM (Pulse Width Modulation) Control

The clock signal coming from OSC has a frequency of 1MHz. When OSC sets the RS latch, the P-Channel MOSFET is turned ON and the N-Channel MOSFET is turned OFF, causing an inductor current I_L to increase. The opposite happens when the current comparator (Current Comp) resets the RS latch i.e. the P-Channel MOSFET is turned OFF and the N-Channel MOSFET is turned ON. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE" which is a voltage proportional to the current I_L and the voltage feedback control signal, FB.

(b) SLLM™ (Simple Light Load Mode) Control

When the control mode is shifted by PWM from heavier load to the one for lighter load or vice versa, the switching pulse is designed to turn OFF with the device held operating in normal PWM control loop. This allows linear operation without voltage drop or deterioration in transient response during sudden load changes. .

Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is designed such that the RESET signal is kept constant when shifted to the light load mode where the switching is tuned OFF and the switching pulses disappear. Activating the switching discontinuously reduces the switching dissipation and improves the efficiency.

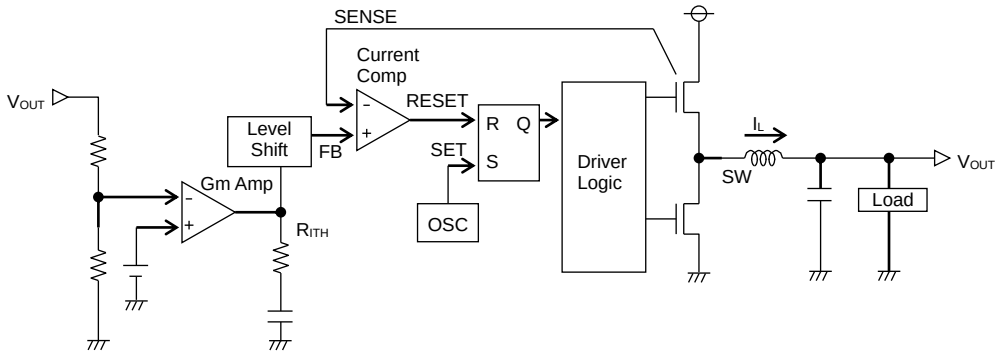


Figure 22. Diagram of Current Mode PWM Control

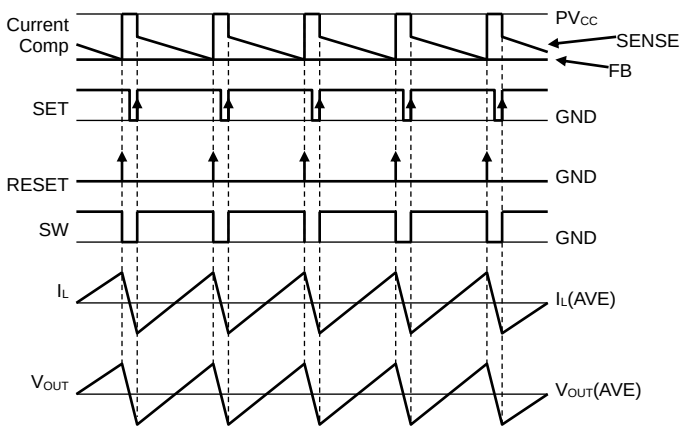


Figure 23. PWM Switching Timing Chart

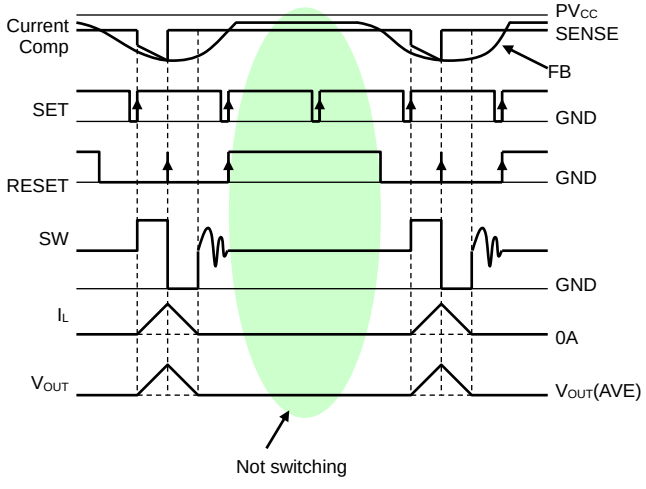


Figure 24. SLLM™ Switching Timing Chart

2. Description of Functions

(1) Soft-Start Function

When EN terminal is shifted to “High” activates a soft-starter to gradually establish the output voltage with the current being limited during startup. It prevents an overshoot of output voltage and an inrush current.

The slope of input signal is different and the soft start time is different depending on the value offset output voltage. When set to 1V ,t_{SS}=1msec(Typ)

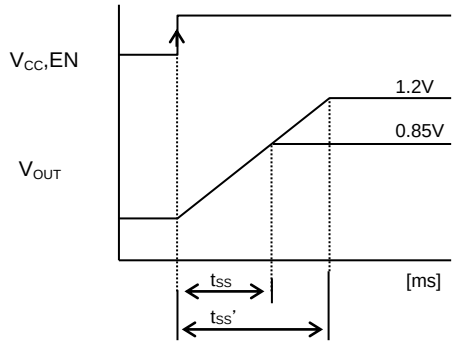


Figure 25. Soft-Start Action

(2) Shutdown Function

When EN terminal is shifted to “Low”, the device turns to Standby Mode, and all the functional blocks including reference voltage circuit, internal oscillator and drivers are turned to OFF. Circuit current during standby is 0μA(Typ).

(3) UVLO Function

It detects whether the input voltage supplied is sufficient to secure the output voltage of this IC. A hysteresis of 50mV (Typ) is designed to prevent output chattering.

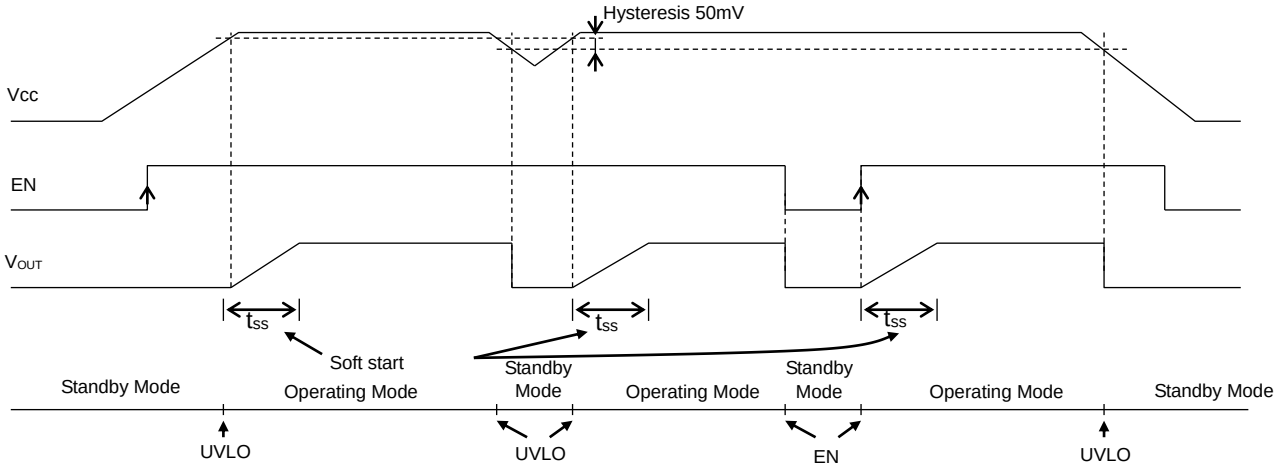


Figure 26. Soft-Start, Shutdown, UVLO Timing Chart

(4) PGOOD Function

When the output voltage falls below 75% (Typ) of a set value, the output of an Open-Drain PGOOD pin is turned OFF. A hysteresis width of 15% (Typ) is designed to prevent output chattering.

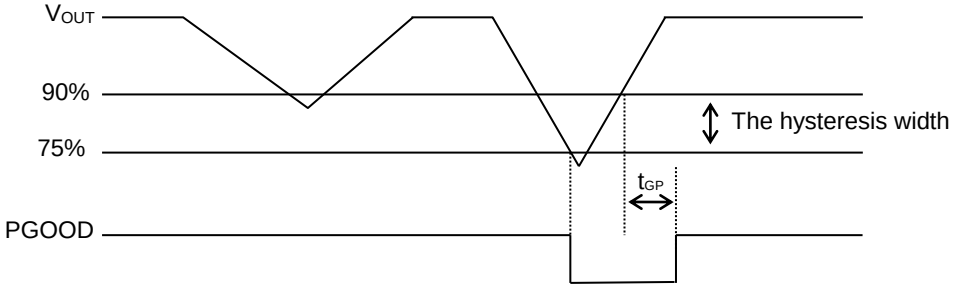
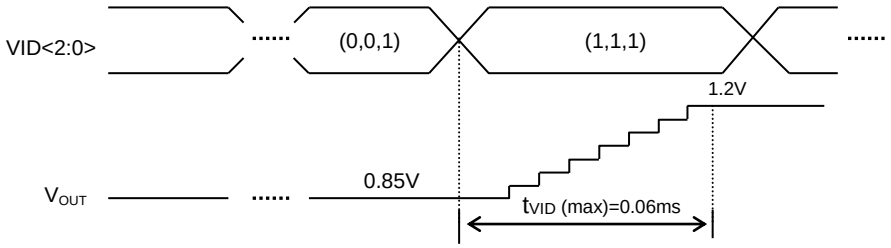


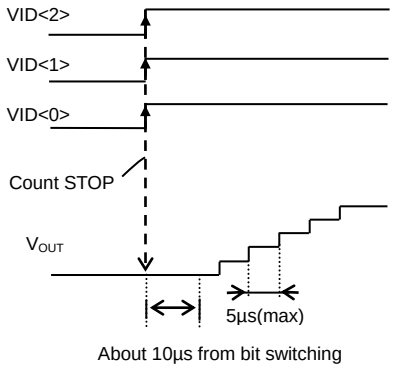
Figure 27. PGOOD Timing Chart

3. About Setting the Output Voltage

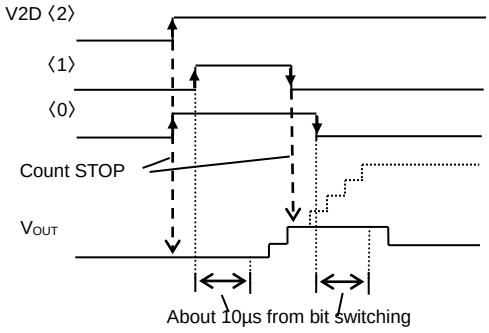
Output voltage shifts step by step as often as bit setting to control the overshoot/undershoot that occurs when changing the of output voltage value. 8 steps (max) delay will occur from the bit switching until output voltage reach to setting value.



(a) Switching 3 bit synchronously



(b) Switching 3 bit with the time lag



(c) Switching 3 bit with the time lag

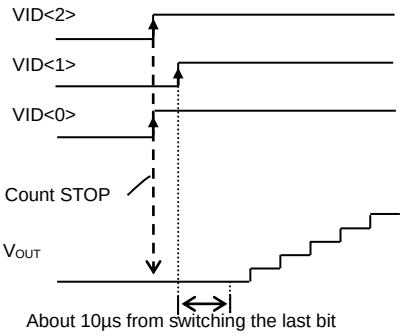


Figure 28. Timing Chart of Setting the Output voltage

It is possible to set output voltage, shown in diagram 1 below, by setting VID<0> to <2> 0 or 1.
VID<2:0> terminal is set to VID<2:0>=(0,0,0) originally by the pull down resistor while in high impedance inside IC.
By pulling up/ pulling down about 10kΩ, the original value can be changed optionally.

Table of output voltage setting

VID<2>	VID<1>	VID<0>	V_{OUT}
0	0	0	1.0V
0	0	1	0.85V
0	1	0	0.9V
0	1	1	0.95V
1	0	0	1.05V
1	0	1	1.1V
1	1	0	1.15V
1	1	1	1.2V

(Note) After 10µs(max) from the bit change, V_{OUT} change starts.
Requiring time for one step (50 mV shift) of V_{OUT} is 5µs(max).
From the bit switching until output voltage reach to setting value, t_{VID}(max)=0.06ms delay will occur.

(1) Short-Current protection circuit with time delay function
It turns OFF the output to protect the IC from breakdown when the incorporated current limiter is activated continuously for the fixed time (t_{LATCH}) or more. The output may be recovered from OFF state by restarting EN or by re-unlocking UVLO.

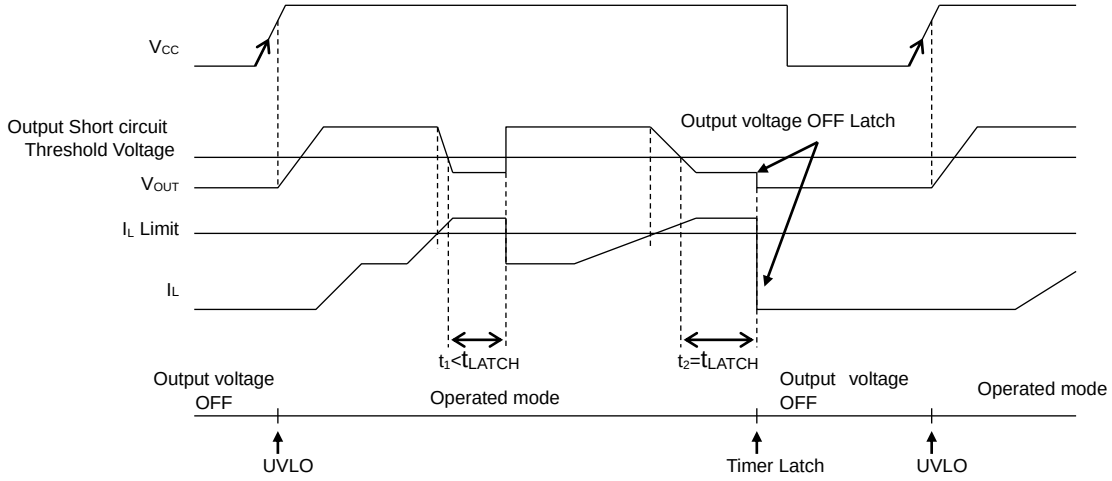


Figure 29. Short-current protection circuit with time delay timing chart

4. Information on Advantages

Advantage 1: Offers fast transient response with current mode control system.

Conventional product (Load response I_O=0.1A to 0.6A) BD9123MUV (Load response I_O=0.6A to 0.1A)

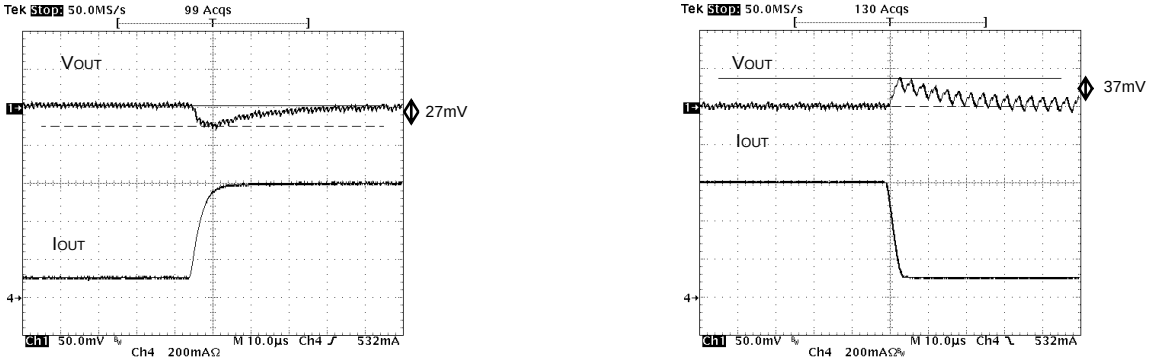


Figure 30. Comparison of Transient Response

Advantage 2: Offers High Efficiency for all Load Range.

(a) For lighter load:
Utilizes the current mode control called SLLM™ for lighter load, which reduces various dissipations such as switching dissipation (P_{SW}), gate charge/discharge dissipation (P_{GATE}), ESR dissipation of output capacitor (P_{ESR}) and ON-Resistance dissipation (P_{RON}) that may otherwise cause degradation in efficiency for lighter load.

↓

Achieves Efficiency Improvement for Lighter Load.

(b) For heavier load:
Utilizes the synchronous rectifying mode and the low ON-Resistance MOS FETs incorporated as power transistor.

{ ON-Resistance of Pch side MOS FET : 0.35mΩ(Typ)
{ ON-Resistance of Nch side MOS FET : 0.25mΩ(Typ)

↓

Achieves Efficiency Improvement for Heavier Load.

Offers high efficiency for all load range with the improvements mentioned above.

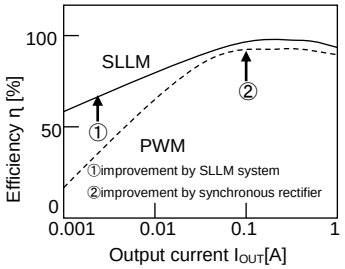


Figure 31. Efficiency

Advantage 3:

(a) Supplied in smaller package due to small-sized power MOS FET incorporated.

- Output capacitor Co required for current mode control: 10µF ceramic capacitor
- Inductor L required for the operating frequency of 1 MHz: 4.7µH inductor

Reduces a Mounting Area Requirement.

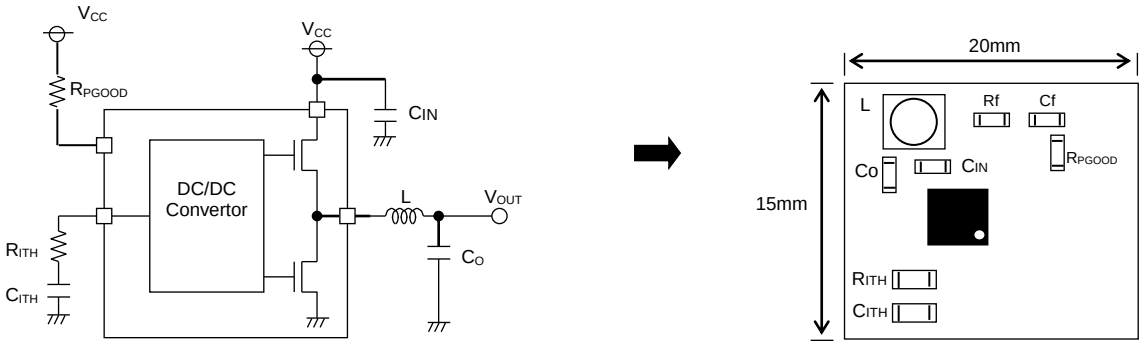


Figure 32. Example of Application

5. Switching Regulator Efficiency

Efficiency η may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times L_{IN}} \times 100 = \frac{P_{OUT}}{P_{IN}} \times 100 = \frac{P_{OUT}}{P_{OUT} + Pd\alpha} \times 100 \quad [\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors Pdα as follows:

Dissipation factors:

(1) ON-Resistance Dissipation of Inductor and FET: Pd(I^2R)

$$Pd(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$$

Where:
R_{COIL} is the DC resistance of inductor.
R_{ON} is the ON-Resistance of FET.
I_{OUT} is the output current.

(2) Gate Charge/Discharge Dissipation: Pd(Gate)

$$Pd(Gate) = C_{gs} \times f \times V^2$$

Where:
C_{gs} is the gate capacitance of FET.
f is the switching frequency.
V is the gate driving voltage of FET.

(3) Switching Dissipation: Pd(SW)

$$Pd(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

Where:
C_{RSS} is the reverse transfer capacitance of FET.
I_{DRIVE} is the peak current of gate.

(4) ESR Dissipation of Capacitor: Pd(ESR)

$$Pd(ESR) = {I_{RMS}}^2 \times ESR$$

Where:
I_{RMS} is the ripple current of capacitor.
ESR is the equivalent series resistance.

(5) Operating Current Dissipation of IC: Pd(IC)

$$Pd(IC) = V_{IN} \times I_{CC}$$

Where:
I_{CC} is the circuit current.

6. Consideration on Permissible Dissipation and Heat Generation

As this IC functions with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the allowable dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON-Resistance of FET are considered. The reason is that the conduction losses are considered to play the leading role among other dissipation mentioned above including gate charge/discharge dissipation and switching dissipation.

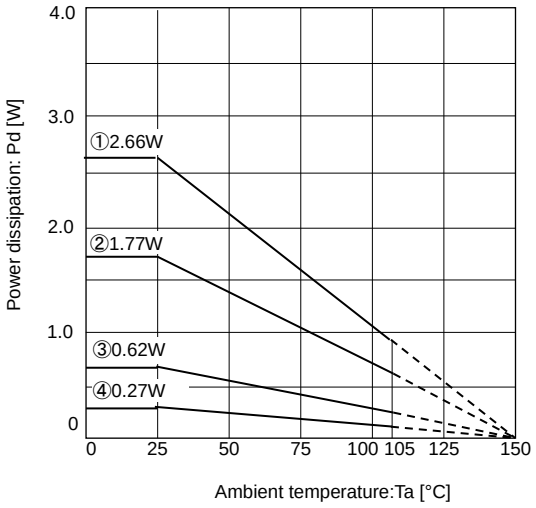


Figure 33. Thermal Derating Curve
(VQFN016V3030)

① 4 layers (Copper foil area : 5505mm^2)
copper foil in each layers.
θj-a=47.0°C/W
② 4 layers (1st and 4th copper foil area : 6.28m^2)
(2nd and 3rd copper foil area: 5505m^2)
(copper foil in each layers)
θj-a=70.62°C/W
③ 1 layer (Copper foil area : 6.28m^2)
θj-a=201.6°C/W
④ IC only.
θj-a=462.9°C/W

$$P = I_{OUT}{}^2 \times R_{ON}$$
$$R_{ON} = D \times R_{ONH} + (1-D)R_{ONL}$$

Where:
D is the ON duty (=V_{OUT}/V_{CC}).
R_{ONH} is the ON-Resistance of Highside MOSFET.
R_{ONL} is the ON-Resistance of Lowside MOSFET.
I_{OUT} is the Output current.

If V_{CC}=5V, V_{OUT}=1.2V, R_{ONP}=0.35mΩ, R_{ONN}=0.25mΩ
I_{OUT}=1.2A, for example,

$D=V_{OUT}/V_{CC}=1.2/5=0.24$

$R_{ON}=0.24x0.35+(1-0.24)x0.25$

$=0.084+0.19$

$=0.274[\Omega]$

$P=1.2^2x0.274=0.394[W]$

As R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON time becomes greater. With the consideration on the dissipation as mentioned above, thermal design must be carried out with sufficient margin allowed.

7. Selection of Components Externally Connected

(1) Selection of Inductor (L)

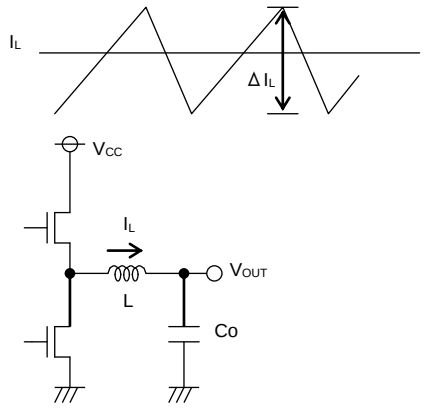


Figure 34. Output ripple current

The inductance significantly depends on output ripple current. As seen in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \quad [A] \quad \cdot\cdot\cdot (1)$$

Appropriate ripple current at output should be 30% more or less of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUTMax} \quad [A] \quad \cdot\cdot\cdot (2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \quad [H] \quad \cdot\cdot\cdot (3)$$

Where:
ΔI_L is the Output ripple current, and
f is the Switching frequency.

Note: Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency. The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.

If V_{CC}=5.0V, V_{OUT}=1.2V, f=1MHz, ΔI_L=0.3x1.2A=0.36A, for example,

$$L = \frac{(5-1.2) \times 1.2}{0.6 \times 5 \times 1M} = 2.53\mu \rightarrow 4.7 \quad [\mu H]$$

Note: Select the inductor with low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

(2) Selection of Output Capacitor (C_O)

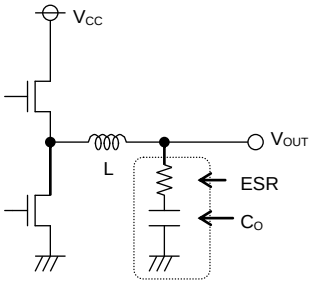


Figure 35. Output Capacitor

Output capacitor should be selected in consideration with the stability region and the equivalent series resistance required to smoothen the ripple voltage.

Output ripple voltage is determined by the equation (4):

$$\Delta V_{OUT} = \Delta I_L \times ESR \quad [V] \quad \cdot\cdot\cdot (4)$$

Where:
ΔI_L is the Output ripple current, and
ESR is the Equivalent series resistance of output capacitor.

Note:Rating of the capacitor should be determined allowing sufficient margin against output voltage. A 10µF to 100µF ceramic capacitor is recommended.

Less ESR allows reduction in output ripple voltage.

(3) Selection of Input Capacitor (C_{IN})

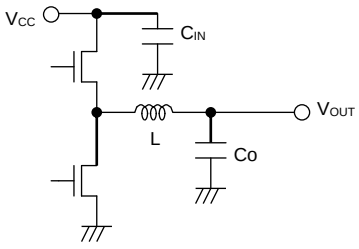


Figure 36. Input Capacitor

The input capacitor to be selected must have sufficiently low ESR to cope with high ripple current to prevent high transient voltage. The ripple current I_{RMS} is given by the equation (5):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \quad [A] \quad \cdot\cdot\cdot (5)$$

< Worst case > I_{RMSMax}

When V_{CC}=2xV_{OUT}, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=1.2V, and I_{OUTMax}=1.2A,

$$I_{RMS} = 1.2 \times \frac{\sqrt{1.2(5-1.2)}}{5} = 0.51 \quad [A_{RMS}]$$

A low ESR 10µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

(4) Determination of R_{ITH}, C_{ITH} that works as a phase compensator

As the Current Mode Control is designed to limit the inductor current, a pole (phase lag) appears in the low frequency area due to a CR filter consists of an output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. So, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

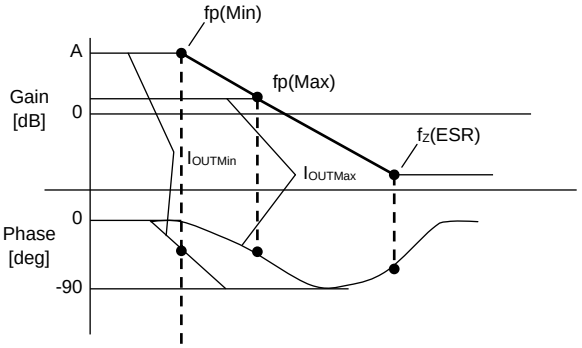


Figure 37. Open Loop Gain Characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$f_{Z(ESR)} = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency lowers.

$$fp_{(Min)} = \frac{1}{2\pi \times R_{OMax} \times C_O} \quad [Hz] \leftarrow with\,lighter load$$

$$fp_{(Max)} = \frac{1}{2\pi \times R_{OMin} \times C_O} \quad [Hz] \leftarrow with\,heavier load$$

Zero at Power Amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR is reduced to half.)

$$f_{Z(Amp)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

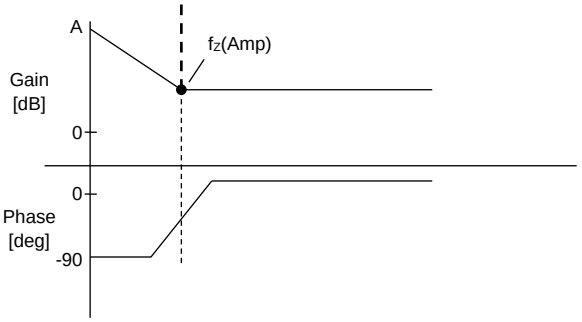


Figure 38. Error Amp Phase Compensation Characteristics

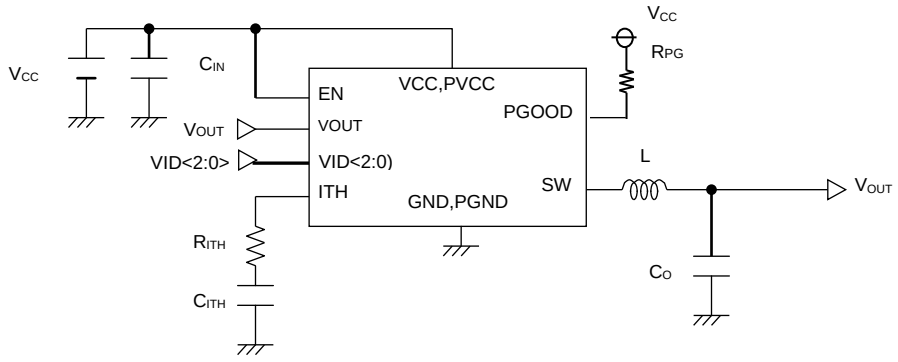


Figure 39. Typical Application

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with CR zero correction by the error amplifier.

$$f_{Z(Amp)} = fp_{(Min)}$$

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{O\,Max} \times C_O}$$

8. Cautions on PC Board Layout

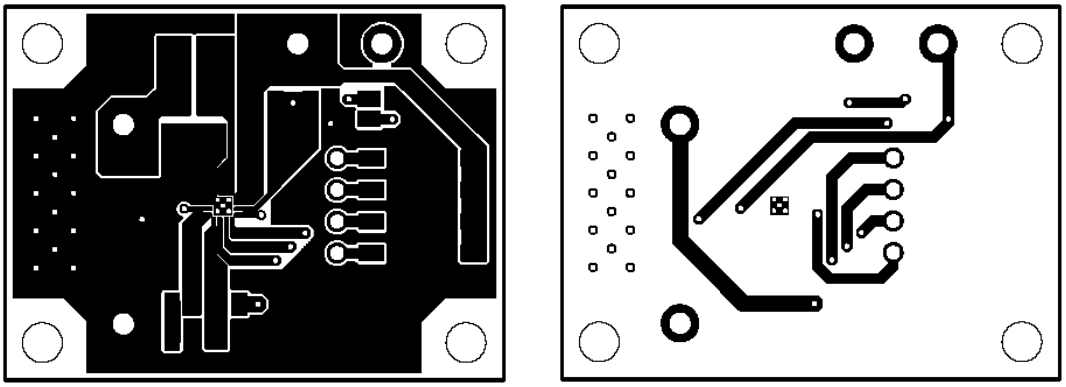


Figure 40. Layout Diagram

(1) Lay out the input ceramic capacitor C_{IN} close to the pins PVCC and PGND, and the output capacitor Co close to pin PGND.
(2) Lay out C_{ITH} and R_{ITH} between the pins ITH and GND as near as possible with least necessary wiring.

Note: VQFN016V3030 has thermal PAD on the reverse of the package.
The package thermal performance may be enhanced by bonding the PAD to GND plane which take a large area of PCB.

9. Recommended Components Lists on Above Application

Symbol	Part	Value	Manufacturer	Series
L	Coil	4.7µH	TDK	VLF5014S-4R7M1R7
C_{IN}	Ceramic Capacitor	10µF	KYOCERA	CM316X5R106M10A
C_O	Ceramic Capacitor	22µF	KYOCERA	CM316B226M06A
C_{ITH}	Ceramic Capacitor	1500pF	Murata	GRM18 Series
R_{ITH}	Resistance	9.1kΩ	ROHM	MCR03 Series
C_f	Ceramic Capacitor	0.1µF	Murata	GRM18 Series
R_f	Resistance	100Ω	ROHM	MCR03 Series

Note: The parts list presented above is an example of recommended parts. Although the parts are standard, actual circuit characteristics should be checked carefully on your application before use. Be sure to allow sufficient margins to accommodate variations between external devices and this IC when employing the depicted circuit with other circuit constants modified. Both static and transient characteristics should be considered in establishing these margins. When switching noise is substantial and may impact the system, a low pass filter should be inserted between the VCC and PVCC pins, and a Schottky Barrier diode or snubber connected between the SW and PGND pins.

I/O Equivalent Circuit

【BD9123MUV】

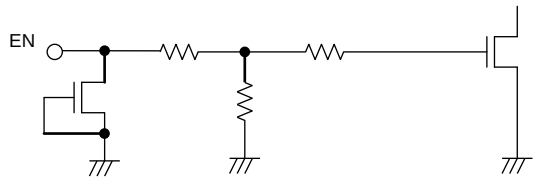
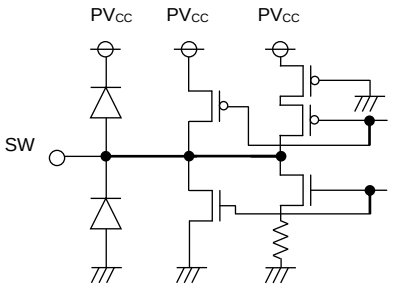
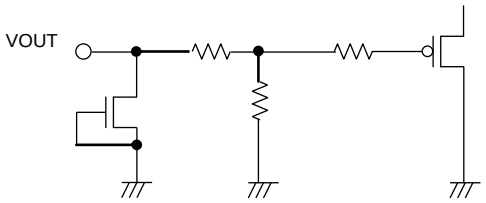
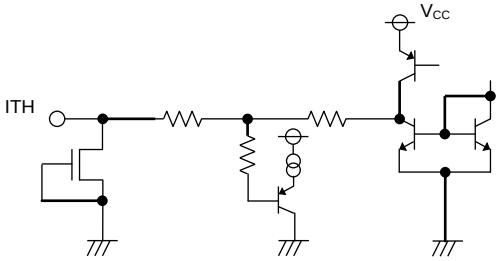
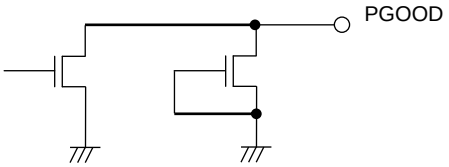
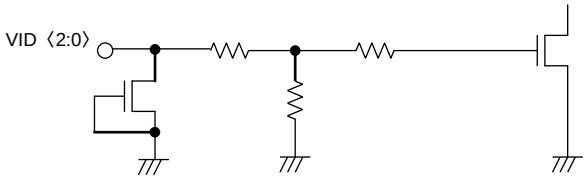
・EN pin	・SW pin
	
・VOUT pin	・ITH pin
	
・PGOOD	・VID〈2:0〉 pin
	

Figure 41. I/O Equivalent Circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

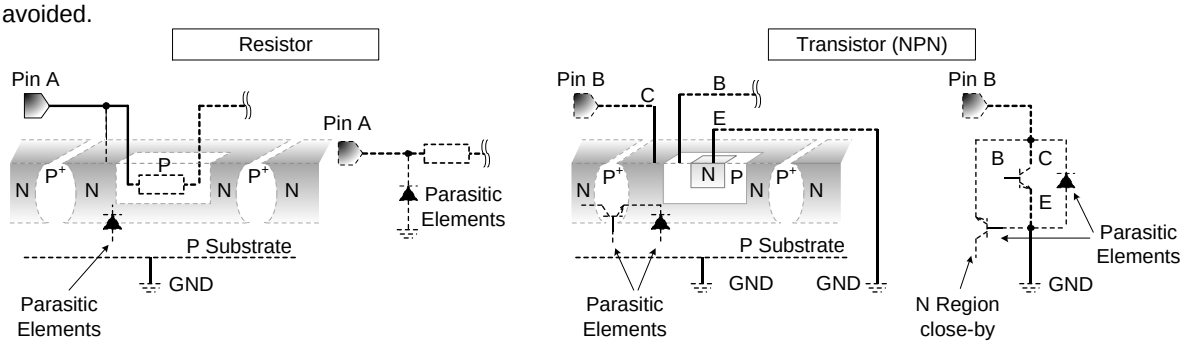


Figure 42. Example of monolithic IC structure

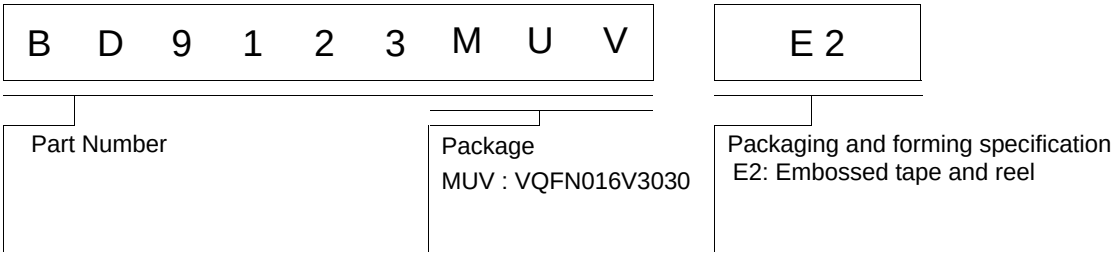
13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

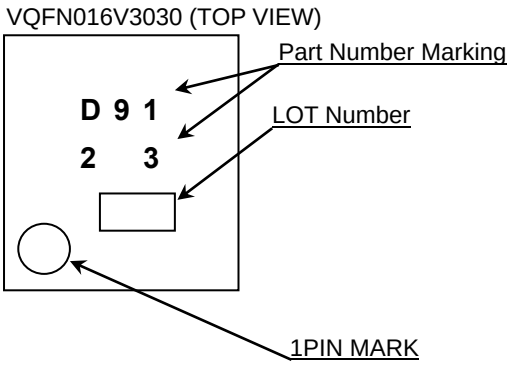
14. Selection of Inductor

It is recommended to use an inductor with a series resistance element (DCR) 0.1Ω or less. Especially, note that use of a high DCR inductor will cause an inductor loss, resulting in decreased output voltage. Should this condition continue for a specified period (soft start time + timer latch time), output short circuit protection will be activated and output will be latched OFF. When using an inductor over 0.1Ω, be careful to ensure adequate margins for variation between external devices and this IC, including transient as well as static characteristics. Furthermore, in any case, it is recommended to start up the output with EN after supply voltage is within.

Ordering Information

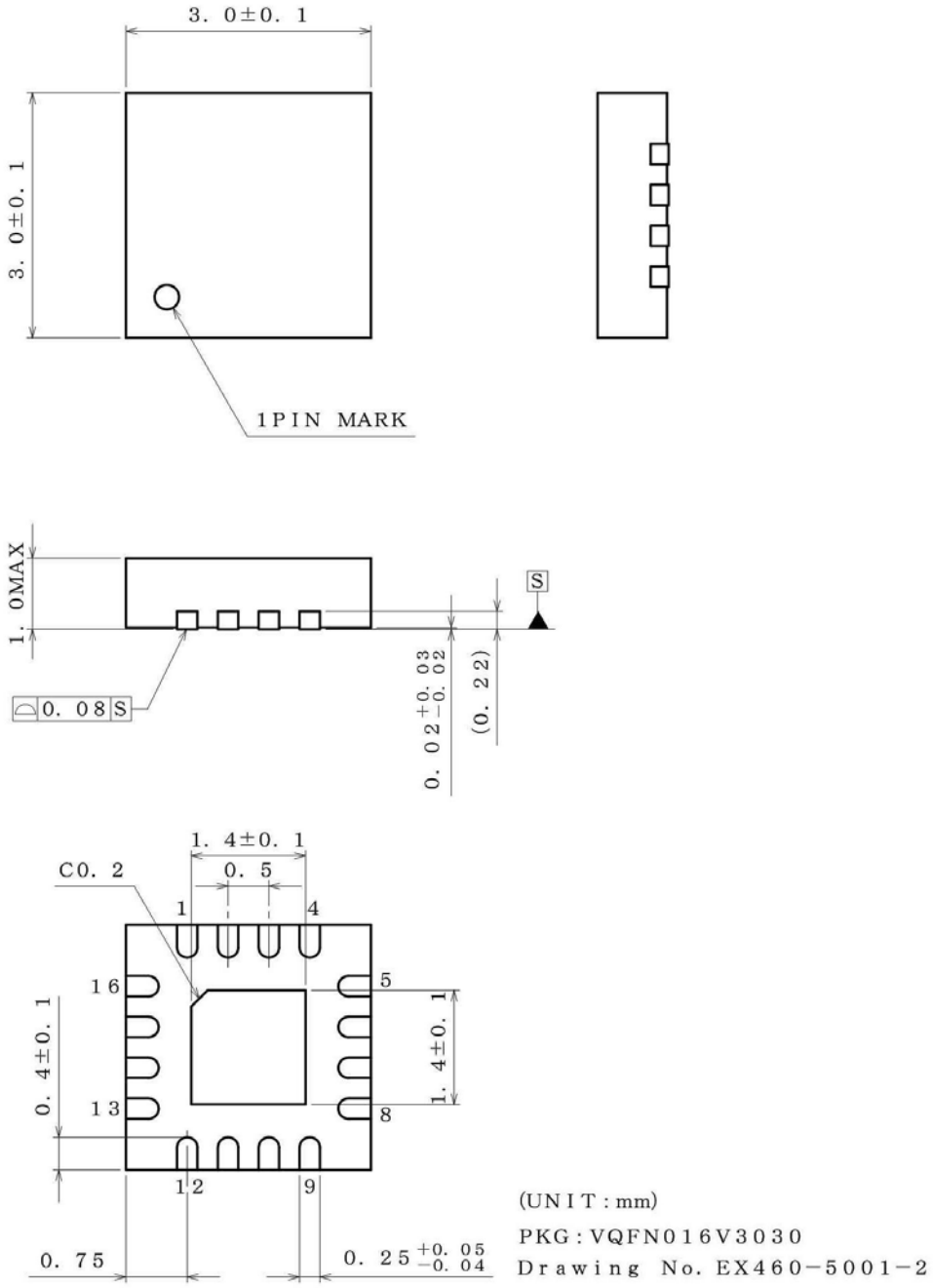


Marking Diagram



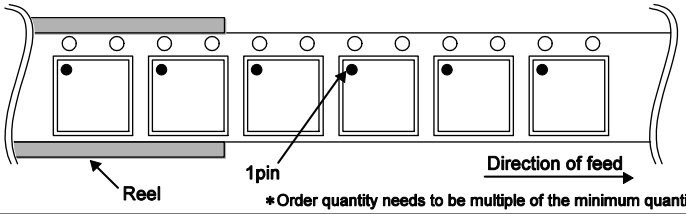
Physical Dimension, Tape and Reel Information

Package Name	VQFN016V3030



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
02.Mar.2012	001	New Release
02.Oct.2014	002	Applied the ROHM Standard Style and improved understandability.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

2. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the information contained in this document.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.