PIC18F45J10 Family
Silicon Errata and Data Sheet Clarification

The PIC18F45J10 family devices that you have received conform functionally to the current Device Data Sheet (DS39682**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F45J10 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F45J10 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
PIC18F24J10	1D0h	1h	3h	3h
PIC18F25J10	1C0h			
PIC18F44J10	1D2h			
PIC18F45J10	1C2h			
PIC18LF24J10	1D4h			
PIC18LF25J10	1C4h			
PIC18LF44J10	1D6h			
PIC18LF45J10	1C6h			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F2XJXX/4XJXX Family Flash Microcontroller Programming Specification"* (DS39687) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
Timer1	16-Bit Counter	1.	In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H buffer does not update when TMR1L is read.	X	X	X
EUSART	Reception	2.	In asynchronous duplex communication, received data can get corrupted if any bit of the TXSTA register is modified during reception.	X	X	X
EUSART	Baud Rate	3.	In Synchronous mode, EUSART baud rates using SPBRG values of '0' and '1' may not function correctly.	X	X	X
EUSART	Buffer	4.	After the last received byte has been read from the EUSART Receive Buffer (RCREG), the value is no longer valid for subsequent read operations.	X	X	X
EUSART	9-Bit	5.	In 9-Bit Asynchronous Full-Duplex Receive mode, received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after RCIDL (BAUDCON<6>) is set.	X	X	X
MSSP	SPI	6.	In SPI mode, the Buffer Full flag bit (BF, SSPxSTAT<0>), the Write Collision Detect bit (WCOL, SSPxCON1<7>) and the Receive Overflow Indicator bit (SSPOV, SSPxCON1<6>) are not reset upon disabling the SPI module.	X	X	X
MSSP	I^2C™	7.	After a Power-on Reset, I^2C mode may not initialize properly if only the SCLx and SDAx pins have been configured as either inputs or outputs.	X	X	X
Core	Program Memory	8.	Writes to program memory address, 300000h, that are not blocked, can cause different locations of the program memory to become corrupted.	X	X	X
EUSART	Transmission	9.	In rare situations, one or more extra zero bytes may appear in packets transmitted with the module in Asynchronous mode.	X	X	X
ECCP	PWM	10.	When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.	X	X	X
MSSP	I^2C™	11.	When configured for I^2C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/ Transmit Buffer Register (SSPBUF) is not read within a window after the SSPxIF interrupt (PIR1<3>) has occurred.	X	X	X
EUSART	Interrupt	12.	In rare situations, unexpected results may occur if interrupts are disabled and enabled and a two-cycle instruction is executed.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Timer1

In 16-Bit Asynchronous Counter mode or 16-Bit Asynchronous Oscillator mode, the TMR1H buffer does not update when TMR1L is read. This issue only affects the reading of the TMR1H registers. The timers increment and set the interrupt flags as expected. The Timer registers can also be written as expected.

Work around

Use the 8-bit mode by clearing the RD16 (T1CON<7>) bit or use the synchronization option by clearing, T1SYNC (T1CON<2>).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: EUSART

In asynchronous duplex communication, the reception can get corrupted if any bit of the TXSTA register is modified during a reception.

Work around

The CSRC (TXSTA<7>) bit should not be set. Though this is a “don’t care” bit in Asynchronous mode, make sure that this bit is not set.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

3. Module: EUSART

In Synchronous mode, EUSART baud rates using SPBRG values of ‘0’ and ‘1’ may not function correctly.

Work around

Use another baud rate configuration to generate the desired baud rate.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: EUSART

After the last received byte has been read from the EUSART Receive Buffer (RCREG), the value is no longer valid for subsequent read operations. The RCREG register should only be read once for each byte received.

Work around

After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL bit (BAUDCON<6>) for a low-to-high transition, or use the EUSART Receive Interrupt Flag (RCIF, PIR1<5>).

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after RCIDL (BAUDCON<6>) is set.

Work around

Only write to TX9D when a reception is not in progress (RCIDL = 1). No interrupt is associated with RCIDL, therefore, it must be polled in software to determine when TX9D can be updated.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

6. Module: MSSP

In SPI mode, the Buffer Full flag bit (BF, SSPxSTAT<0>), the Write Collision Detect bit (WCOL, SSPxCON1<7>) and the Receive Overflow Indicator bit (SSPOV, SSPxCON1<6>) are not reset upon disabling the SPI module (by clearing the SSPEN bit in the SSPxCON1 register).

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, a subsequent write to SSPxBUF will result in a write collision. Also, if a new byte is received, a receive overflow will occur.

Work around

Ensure that if the buffer is full, SSPxBUF is read (thus, clearing the BF flag) and WCOL is clear before disabling the MSSP module. If the module is configured in SPI Slave mode, ensure that the SSPOV bit is clear before disabling the module.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

7. Module: MSSP (I^2C™ Mode)

After a Power-on Reset, the I^2C mode may not initialize properly by just configuring the SCLx and SDAx pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCLx and SDAx pins as outputs by clearing their corresponding TRIS bits.
2. Force SCLx and SDAx low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCLx and SDAx as inputs by setting their TRIS bits.

Once this is done, use the SSPxCON1 and SSPxCON2 registers to configure the proper I^2C mode as before.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

8. Module: Core (Program Memory Space)

Writes to program memory address, 300000h, that are not blocked, can cause the program memory at different locations to be corrupted.

Work around

Do not write to address, 300000h.

If you wish to modify the contents of the Configuration registers:

1. Modify the Configuration Words located at the end of the user memory:
   - For PIC18FX5J10 devices – 7FF4h
   - For PIC18FX4J10 devices – 3FF4h
2. Issue a Reset command.

   This will reload the Configuration registers with the new configuration setting.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

9. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the Transmit Buffer (TXREG) are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to
- The baud rate counter overflows (at the end of the bit period)
- A Stop bit is being transmitted (shifted out of TSR)

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, load TXREG immediately after TXIF is set or wait 1 bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted.

The TXIF bit is set at the beginning of the Stop bit transmission.

If transmission is intermittent, do one of the following:

- Wait for the TRMT bit to be set before loading TXREG
- Use a free timer resource to time the baud period:
  1. Set up the timer to overflow at the end of the Stop bit.
  2. Start the timer when you load the TXREG.

  Do not load the TXREG when the timer is about to overflow.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

10. Module: ECCP (Enhanced PWM)

When switching direction in Full-Bridge PWM mode, the modulated outputs will switch immediately instead of waiting for the next PWM cycle. This may generate unexpected short pulses on the modulated outputs.

Work around

Disable the PWM or set the duty cycle to zero prior to switching directions.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

11. Module: MSSP – I^2C™

When configured for I^2C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer register (SSPBUF) is not read within a window after the SSPIF interrupt (PIR1<3>) has occurred.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPxIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

12. Module: EUSART

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (the SPEN bit, RCSTAx<7> = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed immediately after setting SPEN = 1

Work around

Add a 2 TCY delay after any instruction that re-enables the EUSART module (sets SPEN = 1). See Example 1.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

EXAMPLE 1: RE-ENABLING A EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf RCSTA1, SPEN;or RCSTA2 if EUSART2
nop ;1 Tcy delay
nop ;1 Tcy delay (two total)

;CPU may now execute 2 cycle instructions
```

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39682**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with PIC18FJ Microcontrollers

Section 2.4 Voltage Regulator Pins (VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (VCAP/VDDCORE)

When the regulator is enabled (F devices), a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

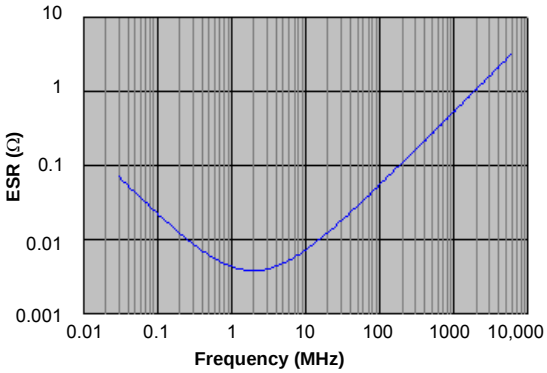
Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 24.0 "Electrical Characteristics"** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 24.0 "Electrical Characteristics"** for information on VDD and VDDCORE.

Note that the "LF" versions of some low pin count PIC18FJ parts (e.g., the PIC18LF45J10) do not have the ENVREG pin. These devices are provided with the voltage regulator permanently disabled; they must always be provided with a supply voltage on the VDDCORE pin.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

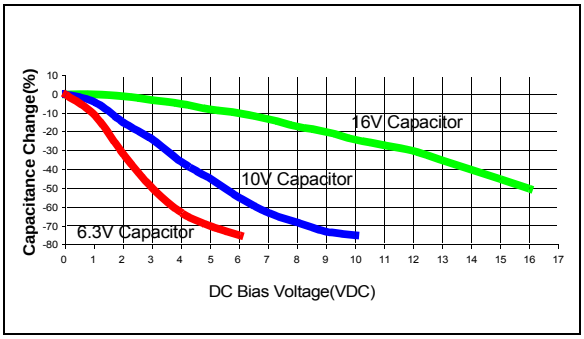
Typical low-cost, 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15%, over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2009)

Combined the issues from the pre-existing A2 and A3 silicon documents, carrying forward silicon issue 1 (Timer1), 2-5 (EUSART), 6 (MSSP), 7 (MSSP – I^2C Mode), 8 (Core – Program Memory Space), 9 (EUSART) and 10 (ECCP – Enhanced PWM). Added issue 11 (MSSP) and 12 (EUSART). Added silicon revision A4.

There were no existing data sheet clarifications to compile into this document. None were added.

This document replaces these errata documents:

- DS80269C, *"PIC18F24J10/25J10/44J10/45J10 Rev. A2 Silicon Errata"*
- DS80380A, *"PIC18F24J10/25J10/44J10/45J10 Rev. A3 Silicon Errata"*

Rev B Document 10/2010)

Added data sheet clarification issue 1 (Guidelines For Getting Started with PIC18FJ Microcontrollers).

NOTES:

Note the following details of the code protection feature on Microchip devices:

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