

# 74F545

## Octal Bidirectional Transceiver with 3-STATE Outputs

### General Description

The 74F545 is an 8-bit, 3-STATE, high-speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24 mA bus drive capability on the A Ports and 64 mA bus drive capability on the B Ports.

One input, Transmit/Receive ( $T/\bar{R}$ ) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A-to-B Ports; Receive enables data from B-to-A Ports. The Output Enable input disables both A and B Ports by placing them in a 3-STATE condition.

### Features

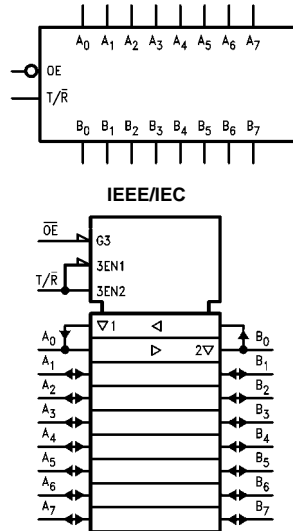
- Higher drive than 8304
- 8-bit bidirectional data flow reduces system package count
- 3-STATE inputs/outputs for interfacing with bus-oriented systems
- 24 mA and 64 mA bus drive capability on A and B Ports, respectively
- Transmit/Receive and Output Enable simplify control logic
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

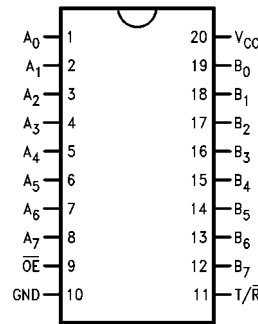
Order Number	Package Number	Package Description
74F545SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F545PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



74F545 Octal Bidirectional Transceiver with 3-STATE Outputs

## Unit Loading/Fan Out

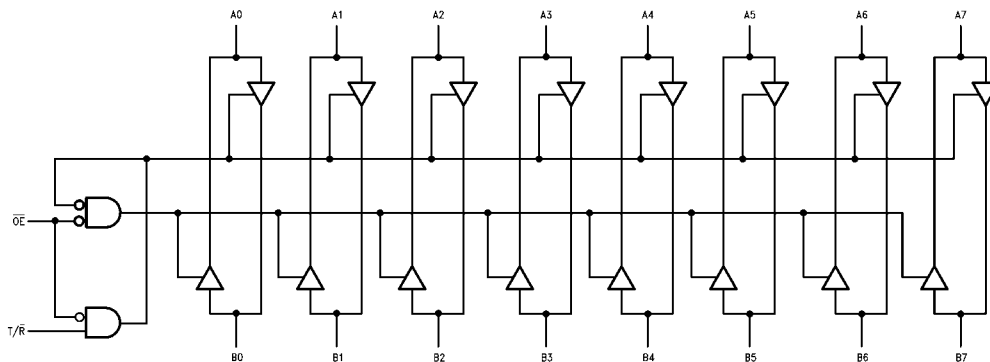
Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/2.0	20 $\mu$ A/-1.2 mA
$\overline{T/R}$	Transmit/Receive Input	1.0/2.0	20 $\mu$ A/-1.2 mA
$A_0$ - $A_7$	Side A 3-STATE Inputs or 3-STATE Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A/-650 $\mu$ A -3 mA/24 mA (20 mA)
$B_0$ - $B_7$	Side B 3-STATE Inputs or 3-STATE Outputs	3.5/1.083 600/106.6 (80)	70 $\mu$ A/-650 $\mu$ A -12 mA/64 mA (48 mA)

## Truth Table

Inputs		Outputs
$\overline{OE}$	$\overline{T/R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

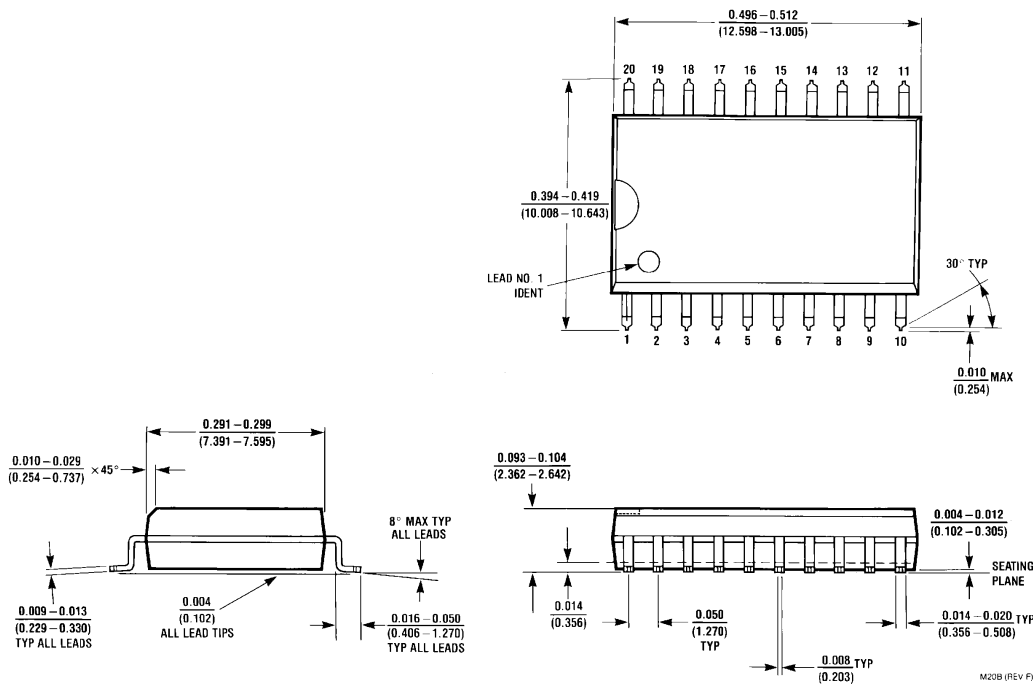
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA ( $\overline{OE}$ , $\overline{TR}$ )
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.0 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> ) I <sub>OH</sub> = -15 mA (B <sub>n</sub> ) I <sub>OH</sub> = -1 mA (A <sub>n</sub> ) I <sub>OH</sub> = -3 mA (A <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub>		0.5 0.55	V	Min	I <sub>OL</sub> = 24 mA (A <sub>n</sub> ) I <sub>OL</sub> = 64 mA (B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V ( $\overline{OE}$ , $\overline{TR}$ )
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V ( $\overline{OE}$ , $\overline{TR}$ )
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEx</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-1.2	mA	Max	V <sub>IN</sub> = 0.5V ( $\overline{OE}$ , $\overline{TR}$ )
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60 -100		-150 -225	mA	Max	V <sub>OUT</sub> = 0V (A <sub>n</sub> ) V <sub>OUT</sub> = 0V (B <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current		70	90	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		95	120	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		85	110	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.5	4.2	6.0	2.0	7.5	2.5	7.0	ns
t <sub>PHL</sub>	A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub>	2.5	4.6	6.0	2.0	7.5	2.5	7.0	
t <sub>PZH</sub>	Output Enable Time	3.0	5.3	7.0	2.5	9.0	3.0	8.0	ns
t <sub>PZL</sub>		3.5	6.0	8.0	3.0	10.0	3.5	9.0	
t <sub>PHZ</sub>	Output Disable Time	3.0	5.0	6.5	2.5	9.0	3.0	7.5	
t <sub>PLZ</sub>		2.0	5.0	6.5	2.0	10.0	2.0	7.5	

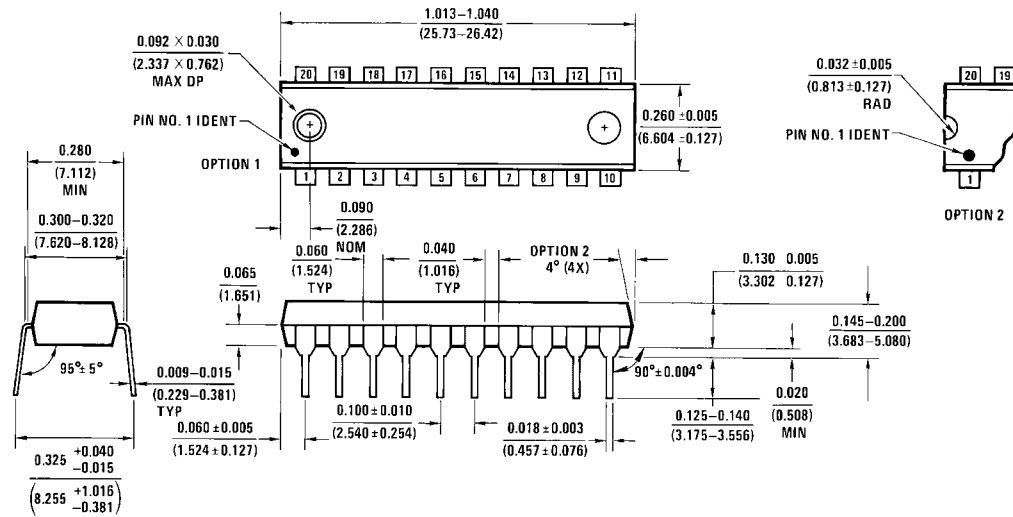
**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**

M20B (REV F)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N20A**

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