Ordering number : EN7739A

LA6571

Monolithic Linear IC

5CH Driver for Mini Disk and Compact Disk

ON Semiconductor®

http://onsemi.com

Overview

The LA6571 is 5-channel driver for mini disk and compact disk applications (BTL-AMP: 5CH).

Features

- Power amplifier 5-channel built-in.
- I_O max 1A
- Level shift circuit built-in.
- Mute circuit (output ON/OFF) with three built-in channels (2-2-1).
  (Operates independently for each of MUTE1: CH1 and 2, MUTE2: CH3 and 4, and MUTE3: CH5.
  Not operating for the regulator (REG))
- Regulator (REG) built-in (external PNP transistor).
  Voltage setting (typ: 1.5V or more) with an external resistor
- Overheat protection circuit (thermal shutdown) built-in.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		14	V
Maximum output current	I_O max	Each output for channel 1 to 5.	1	A
Maximum input voltage	$V_{IN}B$		13	V
MUTE pin voltage	V_{MUTE}		13	V
Allowable loss	Pd max	Independent IC	0.8	W
		Mounted on a specified board*	2	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 76.1mm×114.3mm×1.6mm glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$		4.5 to $V_{CC}2$	V
Supply voltage 2	$V_{CC}2$		6 to 13	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 5V, $V_{CC}2$ = 12V, VREF-IN = 1.65V, unless especially specified

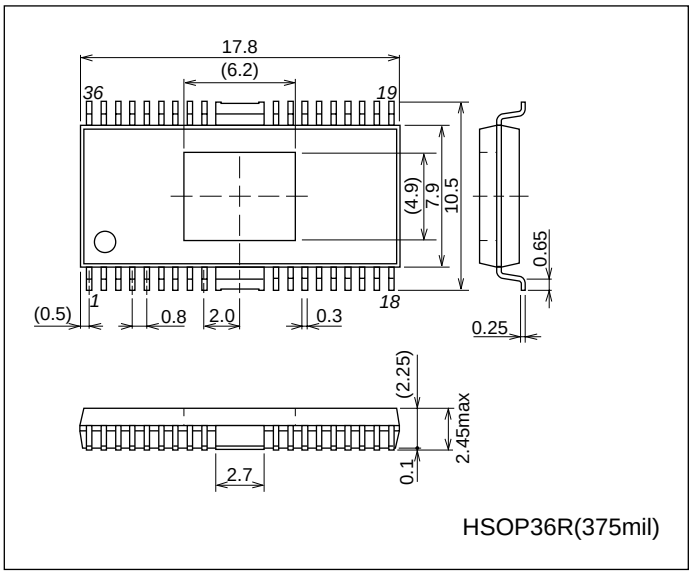
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[ALL Blocks]						
No-load current drain ON	I_{CC} ON	All outputs ON *1		30	50	mA
No-load current drain OFF	I_{CC} OFF	All outputs OFF *1		10	20	mA
VREF input voltage range	VREF-IN		1		$V_{CC}2$-1	V
Thermal shutdown temperature	TSD	*7	150	175	200	°C
[BTL AMP Block] (CH1 to CH5)						
Output offset voltage	V_{OFF}	Voltage difference in output between BTL AMP and each channel.	-50		50	mV
Output offset voltage	$V_{OFF}1$	Voltage difference in output between BTL AMP and each channel.	-80		80	mV
Output voltage	V_O	CH1,CH2 *3	3.2	4.0		V
Output voltage	V_O1	CH3,CH4,CH5 *4	9.7	10.5		V
Closed-circuit voltage gain	V_G1	Gain between input and output for CH1, CH2, and CH5 *2	4.2	5.0	6.0	times
Closed-circuit voltage gain	V_G3	Gain between input and output for CH3 and CH4 *2	8.2	9.0	11.0	times
Slew rate	SR	AMP Independent. Multiply 2 between outputs. *7		0.5		V/μs
MUTE ON voltage	V_{MUTE} ON	Each MUTE *6	2			V
MUTE OFF voltage	V_{MUTE} OFF	Each MUTE *6			0.5	V
[Input AMP Block]						
Input voltage range	V_{IN} op		0		V_{CC}2-1.5	V
Output offset voltage	V_{OFF} op		-10		10	mV
Output current (SINK)	SINK op		2			mA
Output current (SOURCE)	SOURCE op	*5	300	500		μA
[Power Supply Block] (PNP transistor: 2SB632K)						
Regulator output	V_{OUT}	For error Amp, R_L = 10kΩ at buffer	1.2	1.3	1.4	V
REG-IN SINK current	REG-IN-SINK	Base current to external PNP	5	10		mA
Line regulation	ΔV_OLN	6V ≤ V_{CC} ≤ 12V, I_O = 200mA		20	150	mV
Load regulation	ΔV_OLD	5mA ≤ I_O ≤ 200mA		50	200	mV

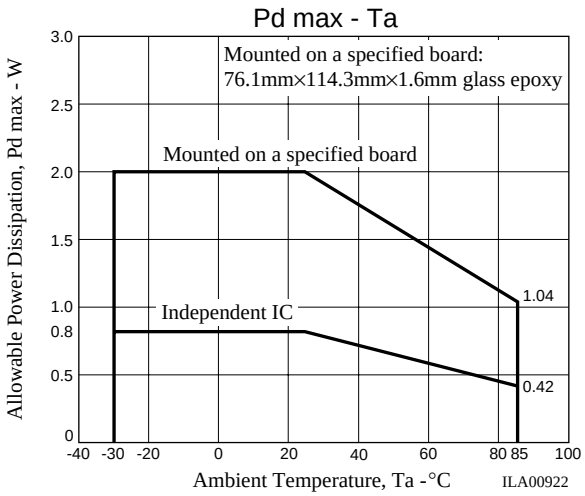
*1. Current dissipation that is a sum of $V_{CC}1$ and $V_{CC}2$ at no load.
*2. Input AMP is a BUFFER AMP.
*3. Voltage difference between both ends of load (8Ω). Output saturated.
*4. Voltage difference between both ends of load (12Ω). Output saturated.
*5. The source of input OP-AMP is a constant current. (See the specified block diagram.)
As the 11kΩ resistance to the next stage is a load, pay due attention when setting the input OP-AMP gain.
*6. Output ON with MUTE: [H] and OFF with MUTE: [L] (HI impedance).
*7. Design guarantee value

Package Dimensions

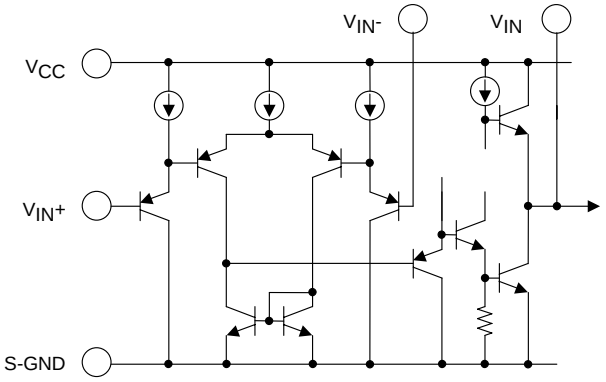
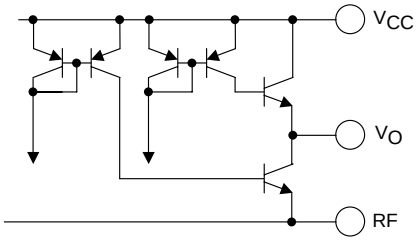
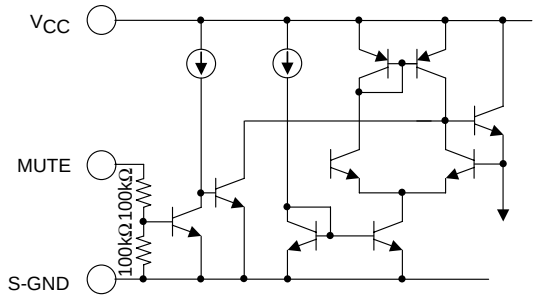
unit : mm

3251

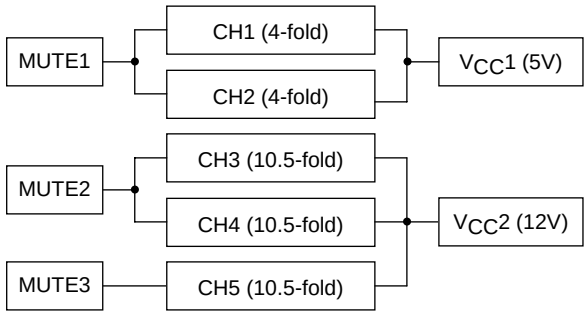




Pin Description

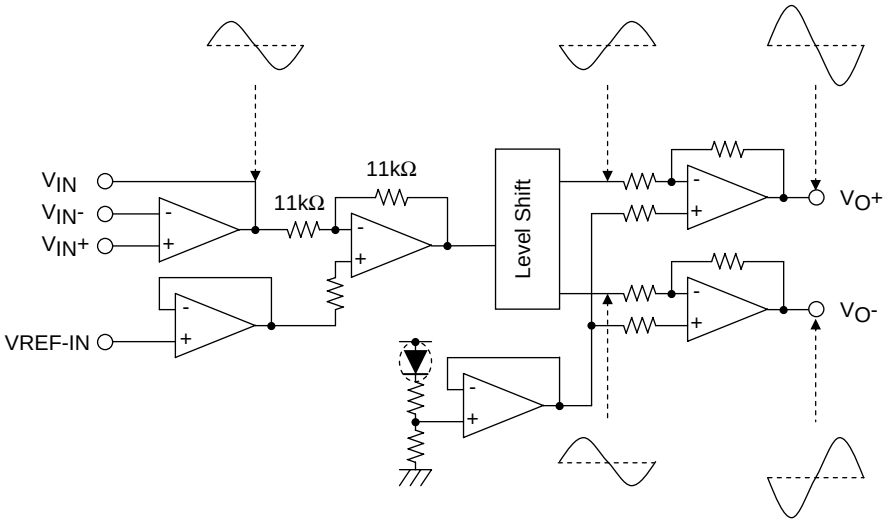
Pin Name	Pin Name	Pin No.	Equivalent Circuit Diagram	Description
Input	$V_{IN}1^+$ $V_{IN}1^-$ $V_{IN}1$ $V_{IN}2^+$ $V_{IN}2^-$ $V_{IN}2$ $V_{IN}3^+$ $V_{IN}3^-$ $V_{IN}3$ $V_{IN}4^-$ $V_{IN}4^+$ $V_{IN}4$ $V_{IN}5^+$ $V_{IN}5^-$ $V_{IN}5$	17 16 15 20 19 18 23 22 21 30 29 31 32 33 34		Each input pin
Output	V_O1^+ V_O1^- V_O2^+ V_O2^- V_O3^+ V_O3^- V_O4^+ V_O4^- V_O5^+ V_O5^-	12 13 10 11 8 9 6 7 5 4		Each output
MUTE	MUTE1 MUTE2 MUTE3	1 2 36		Turns ON/OFF the output for MUTE1: CH1, 2 MUTE2: CH3, 4, and MUTE3: CH5. Each MUTE operates independently. MUTE: H output ON MUTE: L output OFF With the output OFF, the output has a high impedance.

Relationship between MUTE and Power (V_{CC})

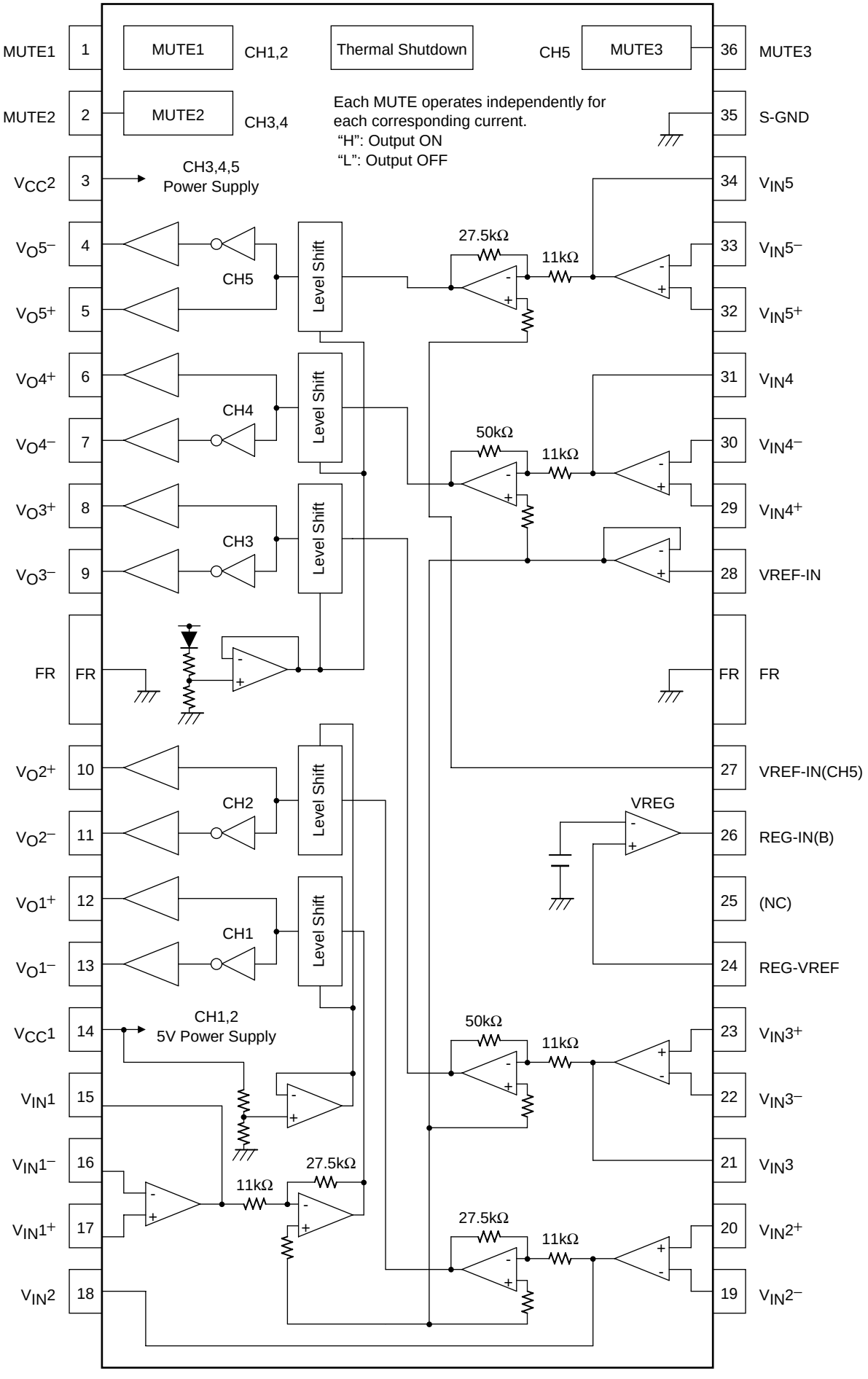


* MUTE operates independently for each corresponding channel.

Schematic Diagram of I/O Related Components



Block Diagram



Sample Application Circuit