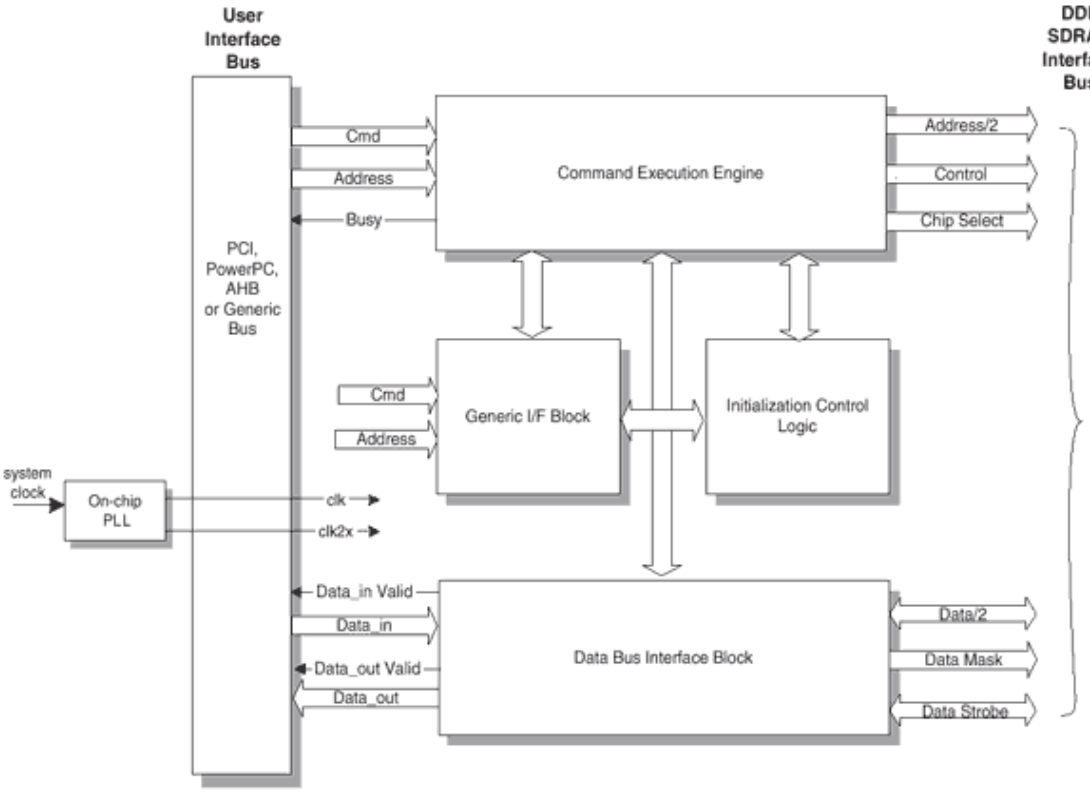
# DDR SDRAM Controller - Pipelined for ispXPGA and ORCA4

## Overview

DDR (Double Data Rate) SDRAM was introduced as a replacement for SDRAM memory running at bus speeds over 75MHz. DDR SDRAM is similar in function to the regular SDRAM but doubles the bandwidth of the memory by transferring data twice per cycle on both edges of the clock signal, implementing burst mode data transfer.

The DDR SDRAM Controller is a parameterized core giving user the flexibility for modifying the data widths, burst transfer rates, and CAS latency settings of the design. In addition, the DDR core supports intelligent bank management, which is done by maintaining a database of "all banks activated" and the "rows activated" in each bank. With this information, the DDR SDRAM Controller decides if an active or pre-charge command is needed. This effectively reduces the latency of read/write commands issued to the DDR SDRAM.




## Features

- Performance of Greater than 100MHz (200 DDR)
- Interfaces to JEDEC Standard DDR SDRAMs
- Supports DDR SDRAM Data Widths of 16, 32 and 64 Bits
- Supports up to 8 External Memory Banks
- Programmable Burst Lengths of 2, 4, or 8
- Programmable CAS Latency of 1.5, 2.0, 2.5 or 3.0
- Byte-level Writing Supported
- Increased Throughput Using Command Pipelining and Bank Management
- Supports Power-down and Self Refresh Modes
- Automatic Initialization
- Automatic Refresh During Nomal and Power-down Modes

Timing and Settings Parameters Implemented as Programmable Registers

Bus Interfaces to PCI Target, PowerPC and AMBA (AHB) Buses Available

Complete Synchronous Implementation

## Evaluation Configurations

**Performance and Resource Utilization for ORCA 4[1]**

| Parameter File | ddrct_gen_o4_1_008.lpc | ddrct_ahb_o4_1_008.lpc |
|---|---|---|
| Core Configuration | Generic I/F | AHB I/F |
| ORCA 4 PFUs[2] | 344 | 560 |
| LUTs | 1359 | 2322 |
| Registers | 1559 | 2451 |
| Dist. RAM[3] | N/A | 18 |
| fMAX (MHz) | 100 (200 DDR) | 100 (200 DDR) |
| External Pins | 239 | 242 |
| SysMEM™ EBRs | N/A | N/A |
| | | |
| Parameter File | ddrct_pci_o4_1_008.lpc | ddrct_ppc_o4_1_008.lpc |
| Core Configuration | PCI I/F | PPC I/F |
| ORCA 4 PFUs[2] | 510 | 492 |
| LUTs | 2024 | 1922 |
| Registers | 2070 | 2170 |
| Dist. RAM[3] | 16 | 18 |
| fMAX (MHz) | 66[4] | 100 (200 DDR) |
| External Pins | 246 | 181 |
| SysMEM™ EBRs | N/A | N/A |

[1] Performance and utilization characteristics are generated using an OR4E022BA352 in ispLEVER™ v.3.0 software except for the AHB configuration 008 which is generated using OR4E042BM416. Synthesized using Synplicity Synplify, v.7.0.3. When using this IP core in a different density, package, speed, or grade within the ORCA Series 4 family, performance may vary slightly.

[2] PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.

[3] Dist. RAM = distributed memory.

[4] Performance for the PCI configuration of this DDR core is limited by the maximum throughput of the PCI 2.2 interface (66MHz).

[5] All parameters are set to their default values as shown in the Data Sheet.

**Performance and Resource Utilization for XPGA[1]**

| Parameter File | ddrct_gen_xp_1_002.lpc | ddrct_ahb_xp_1_002.lpc |
|---|---|---|
| Device | LFX125B-4FH516CES/2X | LFX500B-4FH516CES/2X |
| Core Configuration | Generic I/F | AHB I/F |

| | | |
|---|---|---|
| **ispXPGA PFUs[2]** | 393 | 751 |
| **LUTs** | 1116 | 1928 |
| **Registers** | 910 | 1599 |
| **$f_{MAX}$** | 100 | 100 |
| **External Pins** | 142 | 145 |
| **SysMEM™ EBRs** | N/A | N/A |
| | | |
| **Parameter File** | ddrct_pci_xp_1_002.lpc | ddrct_ppc_xp_1_002.lpc |
| **Device** | LFX500C-4FH516CES/2X | LFX500B-4FH516CES/2X |
| **Core Configuration** | PCI I/F | PPC I/F |
| **ispXPGA PFUs[2]** | 688 | 647 |
| **LUTs** | 1867 | 1670 |
| **Registers** | 1333 | 1392 |
| **$f_{MAX}$** | 66[3] | 100 |
| **External Pins** | 170 | 154 |
| **SysMEM™ EBRs** | N/A | N/A |

[1] Performance and utilization characteristics are generated using the ispXPGA device shown above in ispLEVER v.3.1 software. The evaluation version of this IP core only works on this specific device density, package and speed grade. [2] PFU is a standard logic block of some Lattice devices. For more information, check the data sheet of the device.

[3] Performance for the PCI configuration of this DDR core is limited by the maximum throughput of the PCI 2.2 interface (66MHz).

## Ordering Information

**Part Numbers:**

For ORCA 4:
DDRCT-GEN-O4-N1
DDRCT-PPC-O4-N1
DDRCT-PCI-O4-N1
DDRCT-AHB-O4-N1

For ispXPGA:
DDRCT-GEN-XP-N1
DDRCT-PCI-XP-N1
DDRCT-AHB-XP-N1
DDRCT-PPC-XP-N1

To find out how to purchase the DDR SDRAM Controller - Pipelined IP Core, please contact your **local Lattice Sales Office**.