



THIS SPEC IS OBSOLETE

Spec No: 001-49315

Spec Title: CY7C10612DV33, 16-MBIT (1M X 16) STATIC
RAM

Replaced by: NONE

Features

- High speed
 - $t_{AA} = 10 \text{ ns}$
- Low active power
 - $I_{CC} = 175 \text{ mA}$ at 100 MHz
- Low CMOS standby power
 - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic Power-down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Available in Pb-free 54-pin TSOP II package

Functional Description

The CY7C10612DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, take Chip Enables (\overline{CE}) and Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

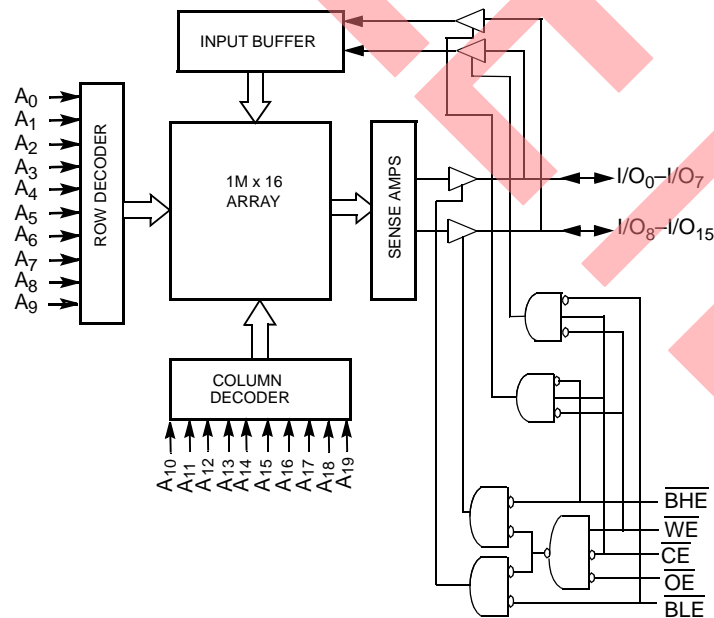
To read from the device, take Chip Enables (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Truth Table on page 10 for a complete description of Read and Write modes.

The input or output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

The CY7C10612DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

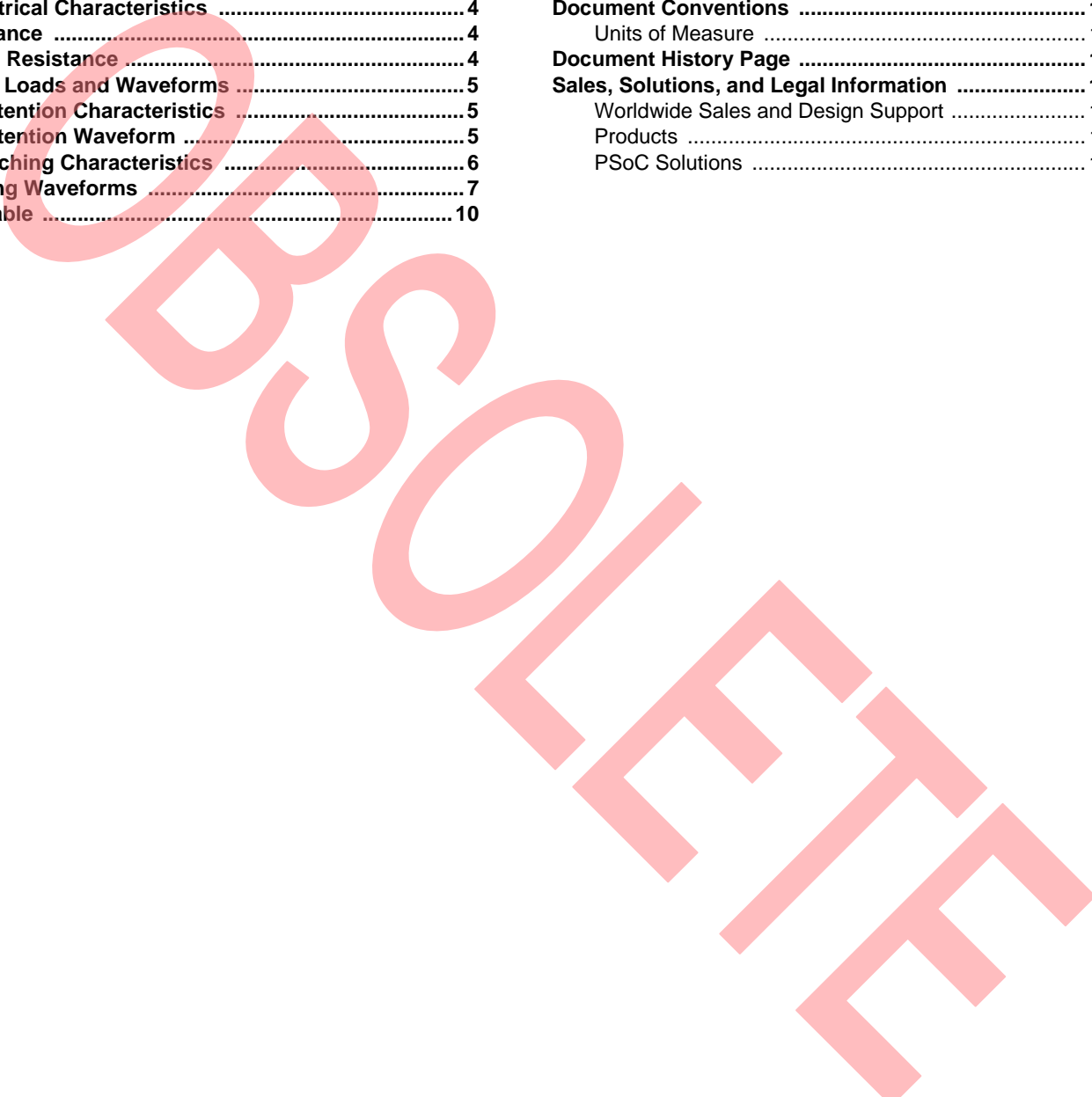
For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

Selection Guide	3	Ordering Information	10
Pin Configuration	3	Ordering Code Definitions	10
Maximum Ratings	4	Package Diagrams	11
Operating Range	4	Acronyms	12
DC Electrical Characteristics	4	Document Conventions	12
Capacitance	4	Units of Measure	12
Thermal Resistance	4	Document History Page	13
AC Test Loads and Waveforms	5	Sales, Solutions, and Legal Information	14
Data Retention Characteristics	5	Worldwide Sales and Design Support	14
Data Retention Waveform	5	Products	14
AC Switching Characteristics	6	PSoC Solutions	14
Switching Waveforms	7		
Truth Table	10		

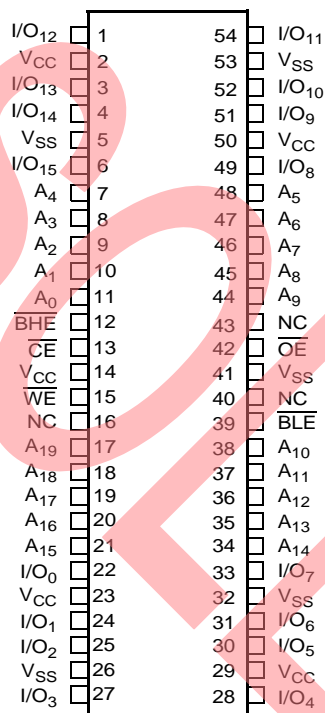


Selection Guide

Description	-10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	175	mA
Maximum CMOS Standby Current	25	mA

Pin Configuration

Figure 1. 54-pin TSOP II (Top View) [1]



Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage on V _{CC} Relative to GND [2]	-0.5 V to +4.6 V
DC Voltage Applied to Outputs in High Z State [2]	-0.5 V to V _{CC} + 0.5 V

DC Input Voltage [2]	-0.5 V to V _{CC} + 0.5 V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		Unit
			Min	Max	
V _{OH}	Output HIGH voltage	Min V _{CC} , I _{OH} = -4.0 mA	2.4	-	V
V _{OL}	Output LOW voltage	Min V _{CC} , I _{OL} = 8.0 mA	-	0.4	V
V _{IH}	Input HIGH voltage		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW voltage [2]		-0.3	0.8	V
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	-1	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _{OUT} ≤ V _{CC} , Output disabled	-1	+1	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = Max, f = f _{MAX} = 1/t _{RC} , I _{OUT} = 0 mA, CMOS levels	-	175	mA
I _{SB1}	Automatic CE power-down current – TTL inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	-	30	mA
I _{SB2}	Automatic CE power-down current – CMOS Inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3 V$, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0	-	25	mA

Capacitance

Parameter [3]	Description	Test Conditions	54-pin TSOP II	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	6	pF
C _{OUT}	I/O capacitance		8	pF

Thermal Resistance

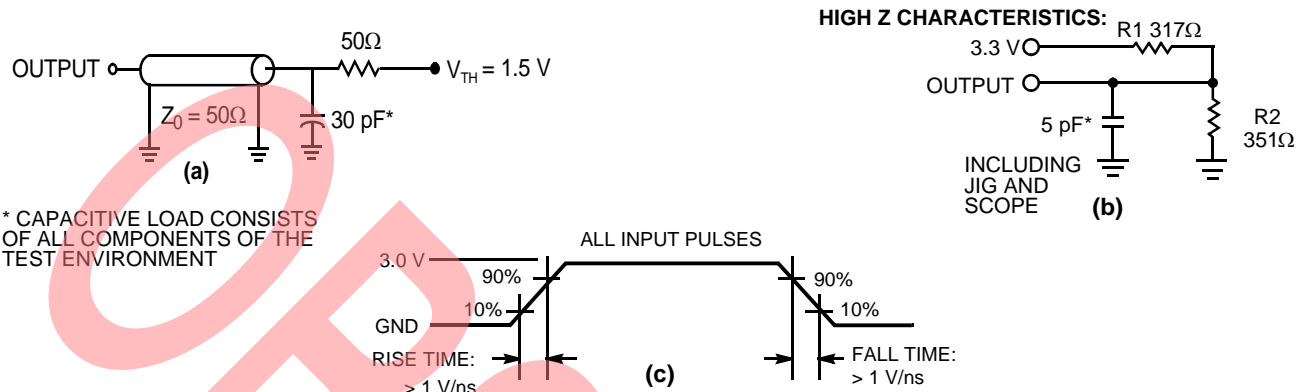
Parameter [3]	Description	Test Conditions	54-pin TSOP II	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	°C/W
θ _{JC}	Thermal resistance (junction to case)		5.40	°C/W

Note

- V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]



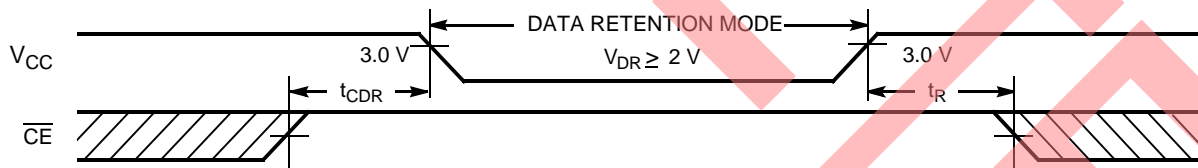
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [5]	Max	Unit
V_{DR}	V_{CC} for data retention		2	—	—	V
I_{CCDR}	Data retention current	$V_{CC} = 2\text{ V}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	—	—	25	mA
$t_{CDR}^{[6]}$	Chip deselect to data retention time		0	—	—	ns
$t_R^{[7]}$	Operation recovery time		t_{RC}	—	—	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 μs (t_{power}) after reaching the minimum operating V_{DD} , normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR} , 2.0 V) voltage.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu\text{s}$ or stable at $V_{CC(min.)} \geq 50\ \mu\text{s}$.

AC Switching Characteristics

Over the Operating Range

Parameter ^[4]	Description	-10		Unit
		Min	Max	
Read Cycle				
t _{power}	V _{CC} (typical) to the first access ^[5]	100	–	μs
t _{RC}	Read cycle time	10	–	ns
t _{AA}	Address to data valid	–	10	ns
t _{OHA}	Data hold from address change	3	–	ns
t _{ACE}	\overline{CE} LOW to data valid	–	10	ns
t _{DOE}	\overline{OE} LOW to data valid	–	5	ns
t _{LZOE}	\overline{OE} LOW to low Z	1	–	ns
t _{HZOE}	\overline{OE} HIGH to high Z ^[6]	–	5	ns
t _{LZCE}	\overline{CE} LOW to low Z ^[6]	3	–	ns
t _{HZCE}	\overline{CE} HIGH to high Z ^[6]	–	5	ns
t _{PU}	\overline{CE} LOW to power-up ^[7]	0	–	ns
t _{PD}	\overline{CE} HIGH to power-down ^[7]	–	10	ns
t _{DBE}	Byte enable to data valid	–	5	ns
t _{LZBE}	Byte enable to low Z	1	–	ns
t _{HZBE}	Byte disable to high Z	–	5	ns
Write Cycle ^[8, 9]				
t _{WC}	Write cycle time	10	–	ns
t _{SCE}	\overline{CE} LOW to write end	7	–	ns
t _{AW}	Address setup to write end	7	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	\overline{WE} pulse width	7	–	ns
t _{SD}	Data setup to write end	5.5	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{LZWE}	\overline{WE} HIGH to low Z ^[6]	3	–	ns
t _{HZWE}	\overline{WE} LOW to high Z ^[6]	–	5	ns
t _{BW}	Byte enable to end of write	7	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of Figure 2 on page 5, unless specified otherwise.
- t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
- t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 2 on page 5. Transition is measured ±200 mV from steady state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$. Chip enable must be active and \overline{WE} and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 2 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [10, 11]

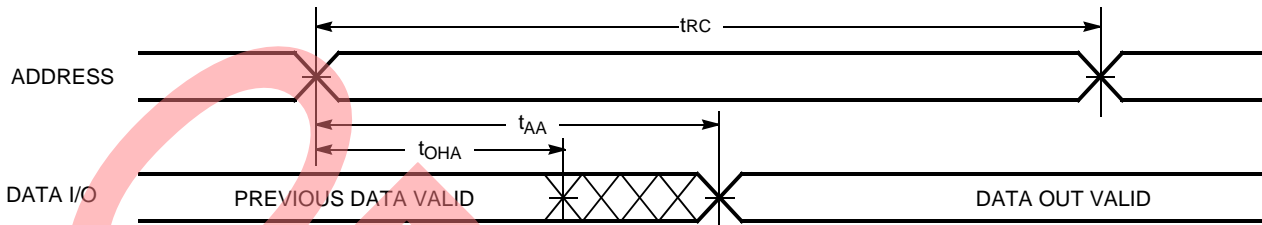
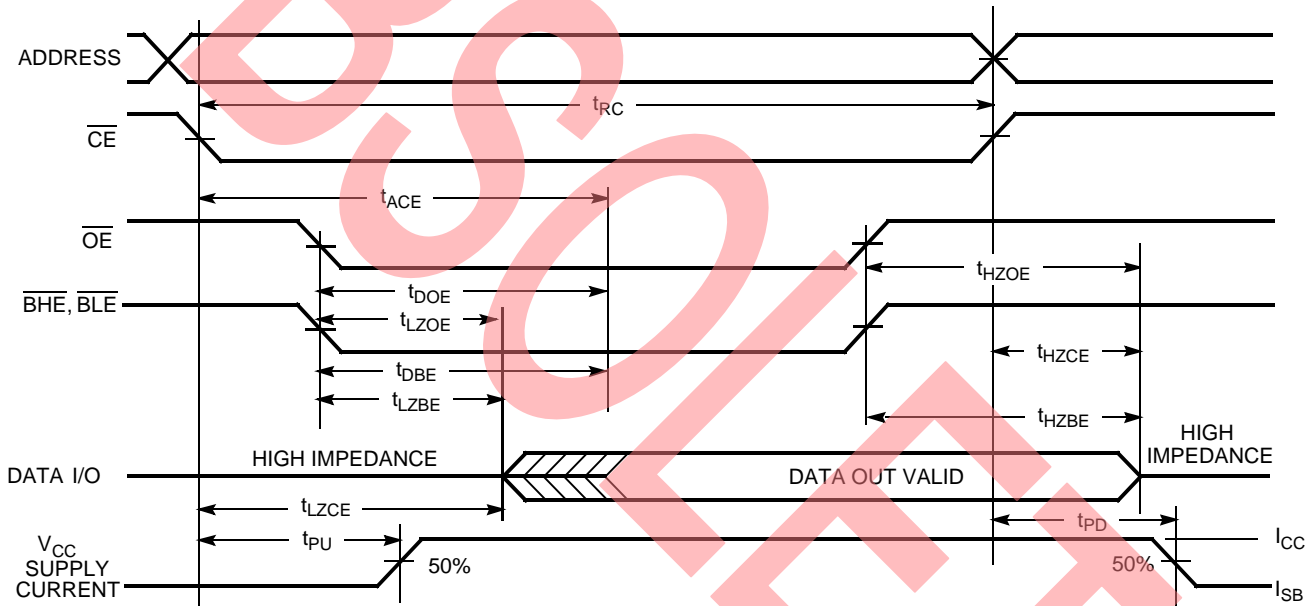


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [11, 12]



Notes

- 10. The device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} , \overline{BHE} , \overline{BLE} or both = V_{IL} .
- 11. \overline{WE} is HIGH for read cycle.
- 12. Address valid before or similar to \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [13, 14]

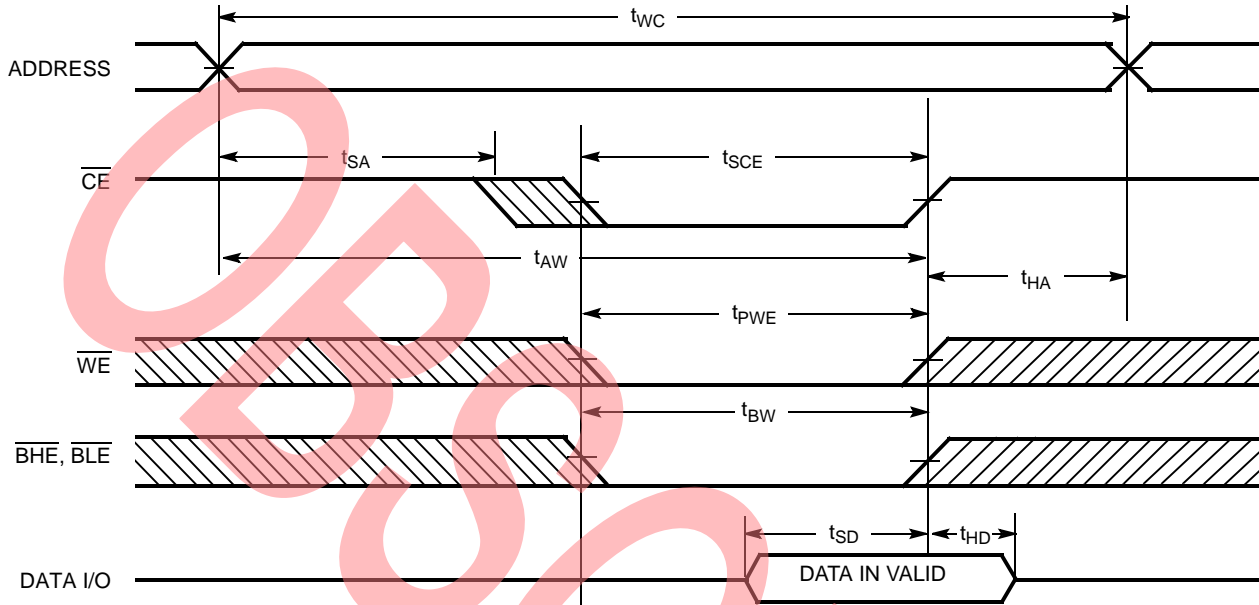
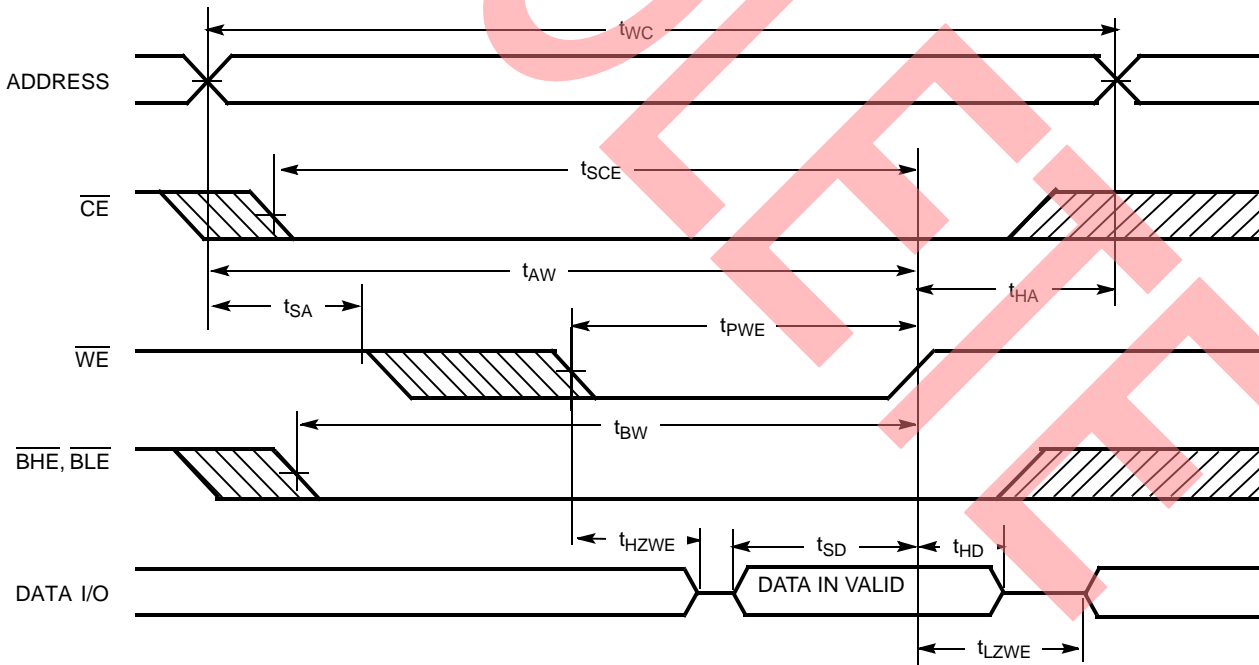


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [13, 14]

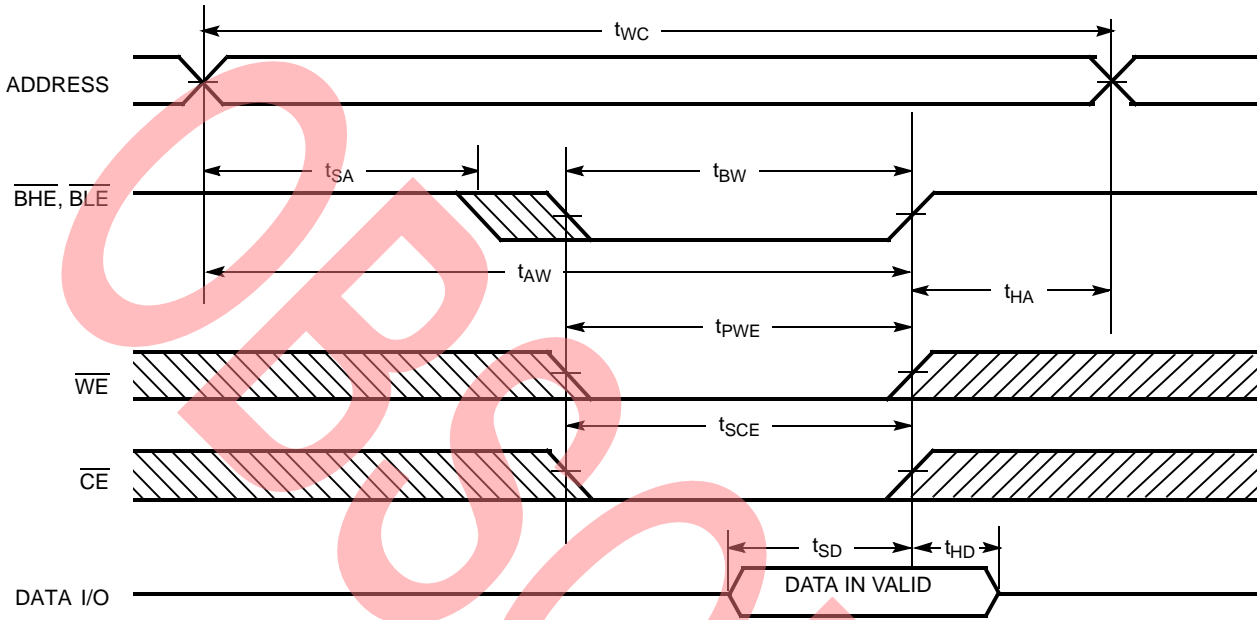


Notes

- 13. Data I/O is high impedance if $\overline{\text{OE}}$, $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
- 14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (BLE or BHE Controlled) [15]



Note

15. Data I/O is high impedance if \overline{OE} , \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

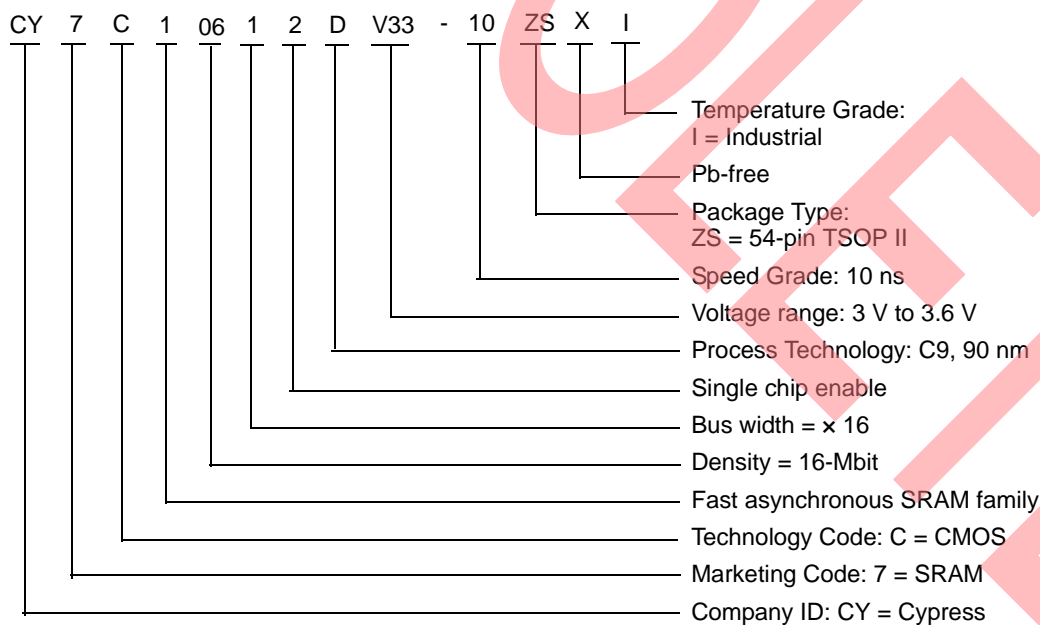
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I _{SB})
L	L	H	L	L	Data Out	Data Out	Read all bits	Active (I _{CC})
L	L	H	L	H	Data Out	High Z	Read lower bits only	Active (I _{CC})
L	L	H	H	L	High Z	Data Out	Read upper bits only	Active (I _{CC})
L	X	L	L	L	Data In	Data In	Write all bits	Active (I _{CC})
L	X	L	L	H	Data In	High Z	Write lower bits only	Active (I _{CC})
L	X	L	H	L	High Z	Data In	Write upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

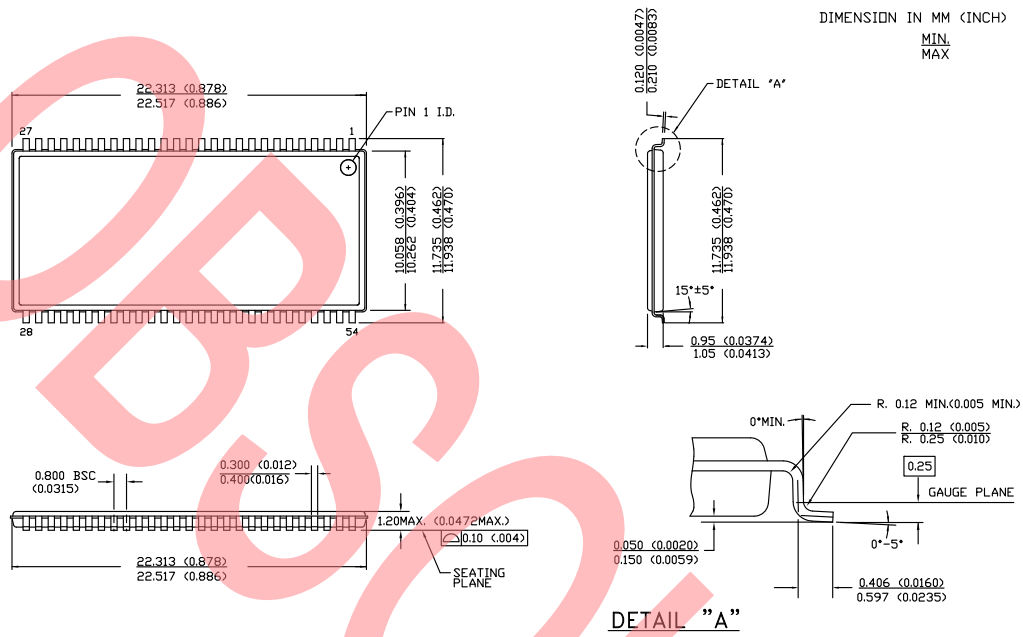
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C10612DV33-10ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagrams

Figure 9. 54-pin TSOP Type II (22.4 x 11.84 x 1.0 mm) Z54-II Package Outline, 51-85160



51-85160 *E

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CE	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C10612DV33, 16-Mbit (1M x 16) Static RAM				
Document Number: 001-49315				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2589743	VKN / PYRS	10/15/08	New data sheet.
*A	2718906	VKN	06/15/09	Post to external web.
*B	3128718	PRAS	01/05/11	Replaced IO with I/O in all instances across the document. Updated Data Retention Characteristics : Added Note 5 and referred the same note in "Typ" column. Added Ordering Code Definitions under Ordering Information . Updated Package Diagrams . Added Acronyms and Units of Measure . Updated to new template.
*C	3412972	TAVA	10/18/2011	Updated Features . Updated DC Electrical Characteristics . Updated Switching Waveforms . Updated Package Diagrams . Updated to new template.
*D	4574311	TAVA	11/19/2014	Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagrams : spec 51-85160 – Changed revision from *C to *E.
*E	5536592	VINI	11/29/2016	Obsolete document. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
	cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

[psoc.cypress.com/solutions](#)

[PSoC 1](#) | [PSoC 3](#) | [PSoC 5](#)

© Cypress Semiconductor Corporation, 2008-2016. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.