

Digital Attenuator 15.5 dB, 5-Bit, TTL Driver, DC-3.5 GHz

Rev. V4

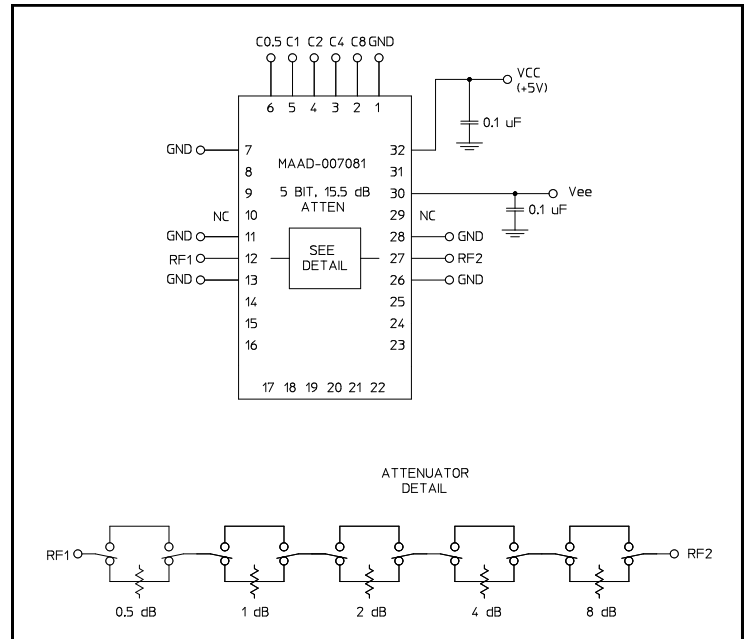
Features

- Attenuation: 0.5 dB Steps to 15.5 dB
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- Test Boards are Available
- Tape and Reel Packaging Available
- Lead-Free CSP-1 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- 260°C Reflow Compatible
- RoHS* Compliant Version of AT90-0283

Description

M/A-COM's MAAD-007081-000100 is a GaAs FET 5-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 15.5 dB total attenuation range. This device is in an PQFN plastic surface mount package. MAAD-007081-000100 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required.

Functional Schematic



Pin Configuration¹

| Pin No. | Function | Pin No. | Function |
|---------|-----------------|---------|-----------------|
| 1 | GND | 17 | NC |
| 2 | C8 | 18 | NC |
| 3 | C4 | 19 | NC |
| 4 | C2 | 20 | NC |
| 5 | C1 | 21 | NC |
| 6 | C0.5 | 22 | NC |
| 7 | GND | 23 | NC |
| 8 | NC | 24 | NC |
| 9 | NC | 25 | NC |
| 10 | NC ² | 26 | GND |
| 11 | GND | 27 | RF2 |
| 12 | RF1 | 28 | GND |
| 13 | GND | 29 | NC ² |
| 14 | NC | 30 | -Vee |
| 15 | NC | 31 | NC |
| 16 | NC | 32 | +Vcc |

Ordering Information

| Part Number | Package |
|--------------------|-------------------|
| MAAD-007081-000100 | Bulk Packaging |
| MAAD-007081-0001TR | 1000 piece reel |
| MAAD-007081-0001TB | Sample Test Board |

Note: Reference Application Note M513 for reel size information.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

1. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)
2. Pins 10 & 29 must be isolated

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Electrical Specifications: $T_A = 25^\circ\text{C}$, $Z_0 = 50\Omega$

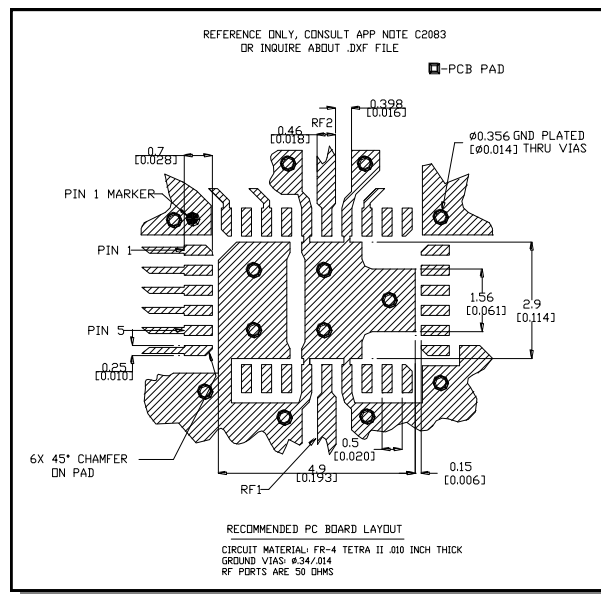
| Parameter | Test Conditions | Frequency | Units | Min | Typ | Max |
|---|--|---------------|--------------------|------|-------|-----------------------------------|
| Insertion Loss | — | DC - 3.5 GHz | dB | — | 2.8 | 3.2 |
| Attenuation Accuracy | Individual Bits 0.5-1-4-8 dB Individual Bit 2 dB Any Combination of Bits 1 to 15.5 dB | DC - 3.5 GHz | dB | — | — | $\pm(.3 + 5\%$ of atten setting) |
| | | DC - 3.5 GHz | dB | — | — | $\pm(.4 + 10\%$ of atten setting) |
| | | DC - 3.5 GHz | dB | — | — | $\pm(.5 + 7\%$ of atten setting) |
| VSWR | Full Range | DC - 3.5 GHz | Ratio | — | 1.6:1 | 1.8:1 |
| Switching Speed | 50% Cntl to 90%/10% RF 10% to 90% or 90% to 10% | — | ns | — | 75 | 150 |
| | | — | ns | — | 20 | 50 |
| 1 dB Compression | — | 50 MHz | dBm | — | +21 | — |
| | | 0.5 - 3.5 GHz | dBm | — | +29 | — |
| Input IP_3 | Two-tone inputs up to +5 dBm | 50 MHz | dB | — | +35 | — |
| | | 0.5-3.5 GHz | dB | — | +48 | — |
| V_{CC} | — | — | V | 4.75 | 5.0 | 5.25 |
| V_{EE} | — | — | V | -8.0 | -5.0 | -4.75 |
| V_{IL} | LOW-level input voltage | — | V | 0.0 | — | 0.8 |
| V_{IH} | HIGH-level input voltage | — | V | 2.0 | — | 5.0 |
| I_{in} (Input Leakage Current) | $V_{in} = V_{CC}$ or GND | — | μA | -1.0 | — | 1.0 |
| I_{CC} (Quiescent Supply Current) | $V_{cntrl} = V_{CC}$ or GND | — | μA | — | 250 | 400 |
| ΔI_{CC} (Additional Supply Current Per TTL Input Pin) | $V_{CC} = \text{Max}$, $V_{cntrl} = V_{CC} - 2.1 \text{ V}$ | — | mA | — | — | 1.0 |
| I_{EE} | V_{EE} min to max, $V_{in} = V_{IL}$ or V_{IH} | — | mA | -1.0 | -0.2 | — |
| Thermal Resistance θ_{jc} | — | — | $^\circ\text{C/W}$ | — | 15 | — |

Absolute Maximum Ratings ^{3,4}

| Parameter | Absolute Maximum |
|---|---|
| Max. Input Power 0.05 GHz 0.5 - 3.5 GHz | +27 dBm +34 dBm |
| V_{CC} | $-0.5V \leq V_{CC} \leq +7.0V$ |
| V_{EE} | $-8.5V \leq V_{EE} \leq +0.5V$ |
| $V_{CC} - V_{EE}$ | $-0.5V \leq V_{CC} - V_{EE} \leq 14.5V$ |
| V_{in}^5 | $-0.5V \leq V_{in} \leq V_{CC} + 0.5V$ |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -65°C to +125°C |

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Recommended PCB Configuration ⁶



- Application Note C2083 is available on line at www.macom.com

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

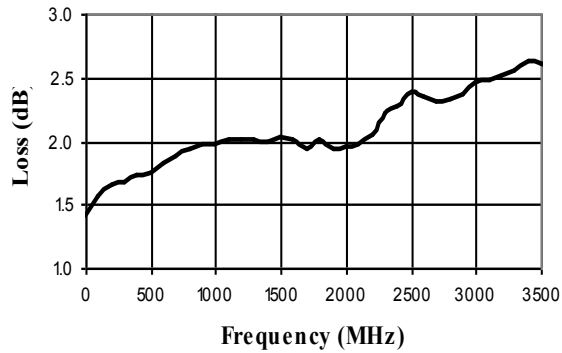
Truth Table (Digital Attenuator)

| C8 | C4 | C2 | C1 | C0.5 | Attenuation |
|----|----|----|----|------|-----------------|
| 0 | 0 | 0 | 0 | 0 | Loss, Reference |
| 0 | 0 | 0 | 0 | 1 | 0.5 dB |
| 0 | 0 | 0 | 1 | 0 | 1.0 dB |
| 0 | 0 | 1 | 0 | 0 | 2.0 dB |
| 0 | 1 | 0 | 0 | 0 | 4.0 dB |
| 1 | 0 | 0 | 0 | 0 | 8.0 dB |
| 1 | 1 | 1 | 1 | 1 | 15.5 dB |

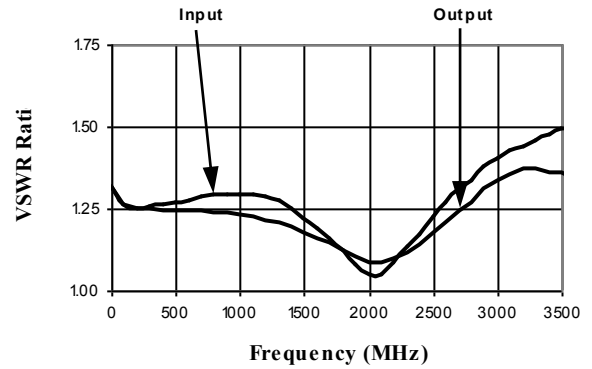
0 = TTL Low; 1 = TTL High

Typical Performance Curves

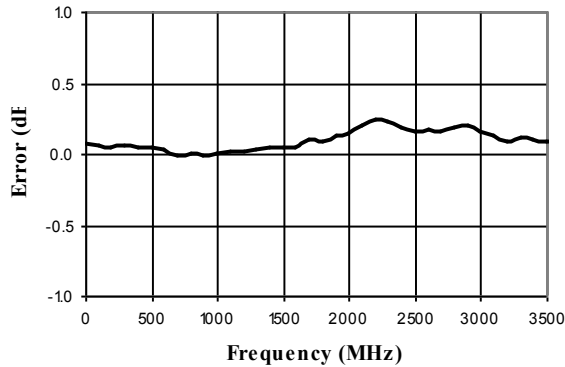
Insertion Loss



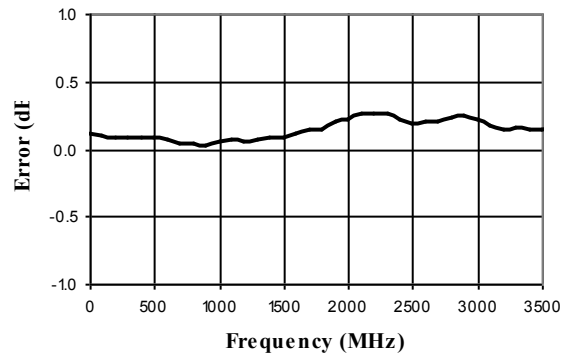
VSWR @ Insertion Loss



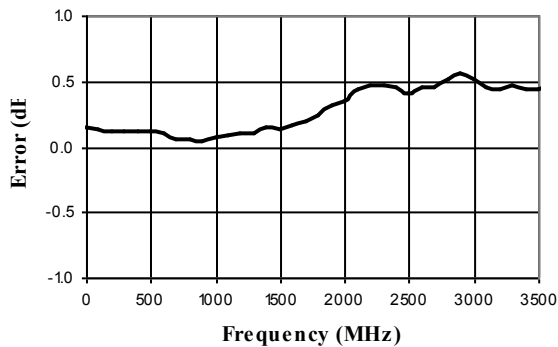
Attenuation Error, 0.5 dB Bit



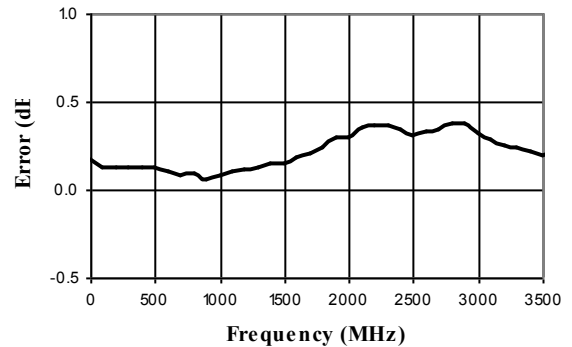
Attenuation Error, 1 dB Bit



Attenuation Error, 2 dB Bit

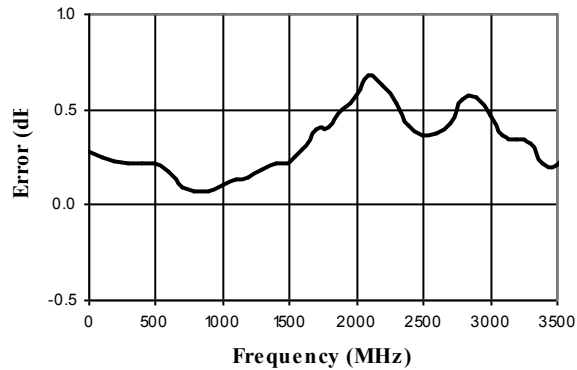


Attenuation Error, 4 dB Bit

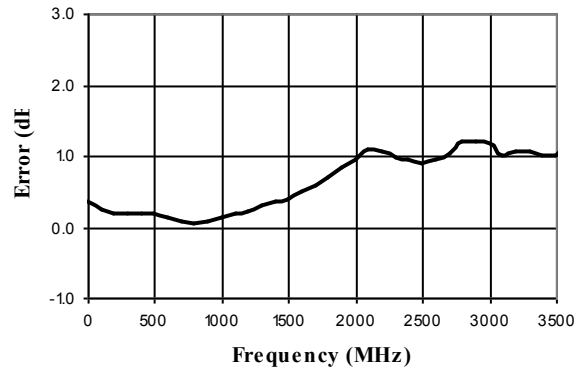


Typical Performance Curves

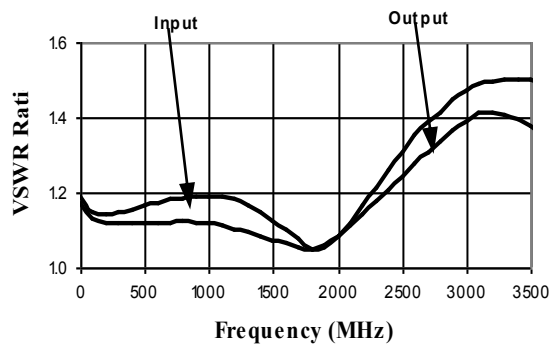
Attenuation Error, 8 dB Bit



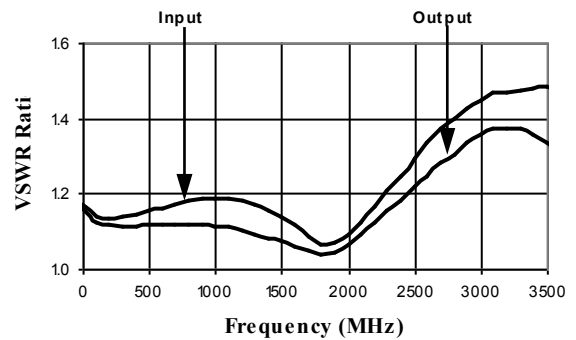
Attenuation Error, Max. Attenuation



VSWR, 0.5 dB Bit

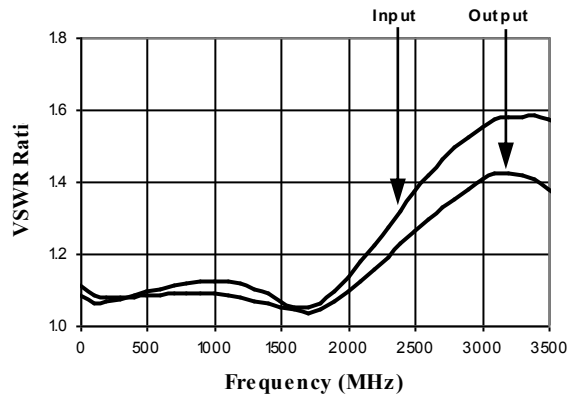


VSWR, 1 dB Bit

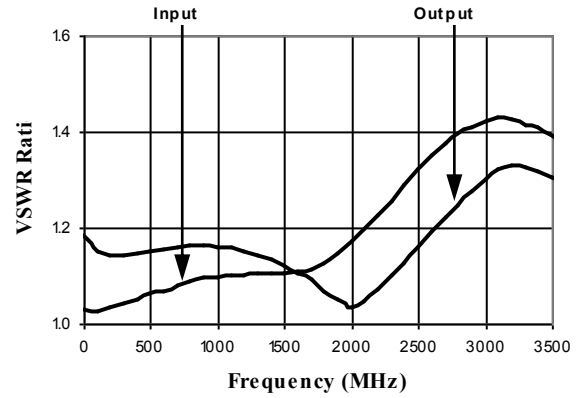


Typical Performance Curves

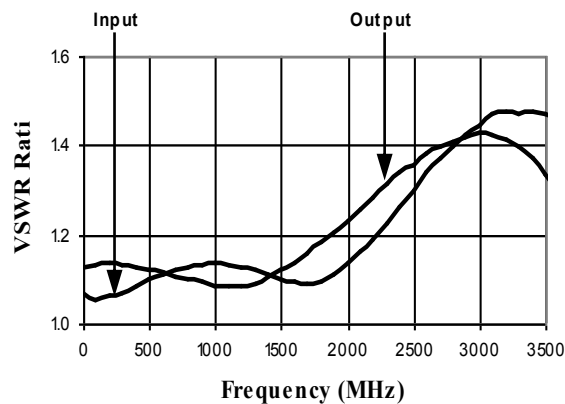
VSWR, 2 dB Bit



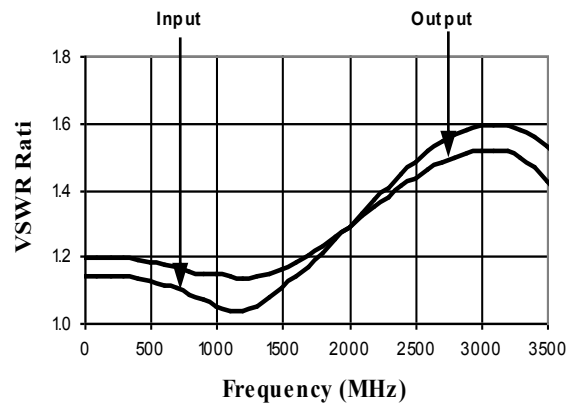
VSWR, 4 dB Bit



VSWR, 8 dB Bit



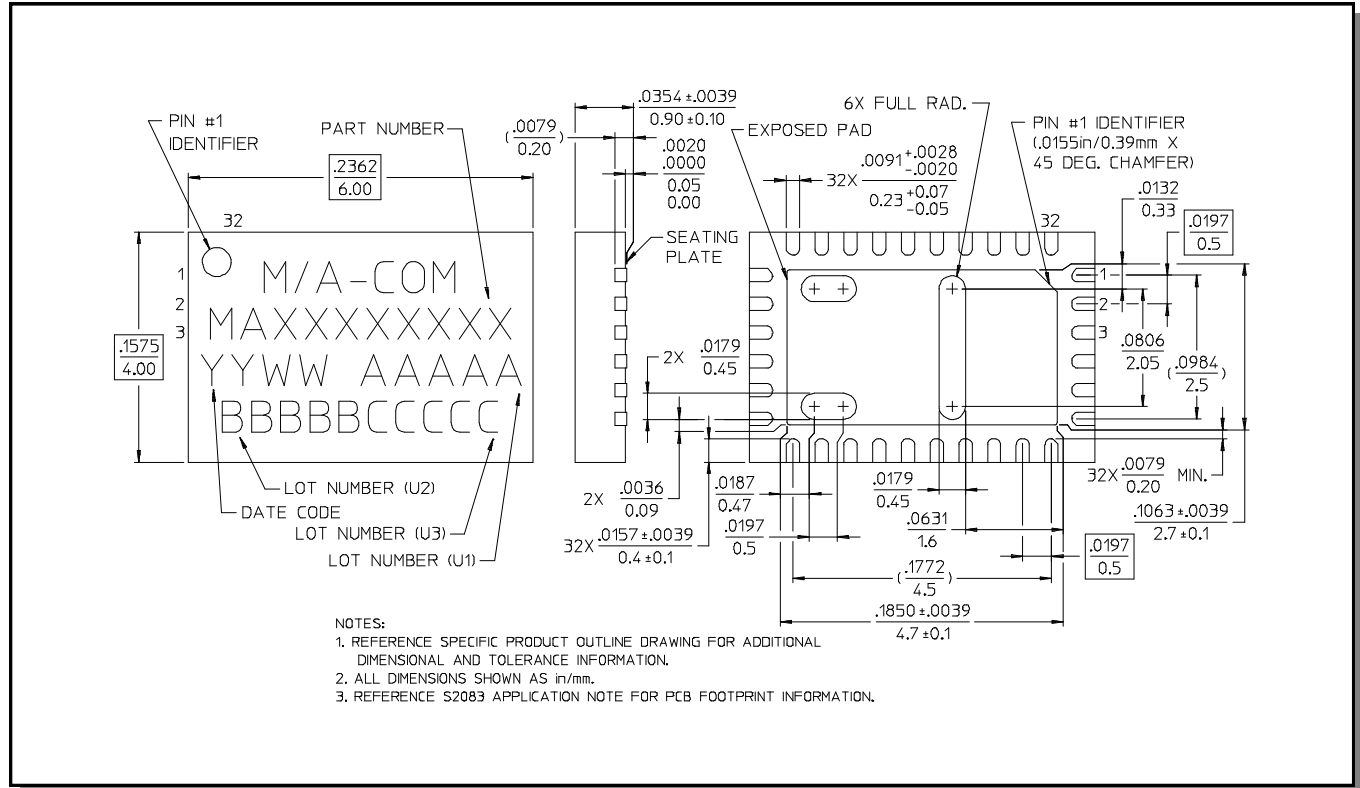
VSWR, Maximum Attenuation



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CSP-1, Lead-Free 4 x 6 mm, 32-lead
PQFN†



† Reference Application Note M538 for lead-free solder reflow recommendations.

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