User Guide for

FEBFSQ500L_H257v1

Evaluation Board

Compact, Green-Mode Controller FSQ500L
5.1 V / 400 mA Flyback Design

Featured Fairchild Product:

FSQ500L

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This user guide supports the evaluation kit for the FSQ500L. It should be used in conjunction with the FSQ500L datasheet as well as Fairchild's application notes and technical support team. Please visit Fairchild's website at www.fairchildsemi.com.

1. Introduction

This engineering report describes a 2.04 W power supply using a FSQ500L. This power supply is targeted for a flyback converter replaces linear power supplies with low cost and small size.

1.1. General Description

This device combines a current-mode Pulse Width Modulator (PWM) with a SenseFET and high-voltage regulator connected from the DRAIN pin to supply the V_{CC}. This device does not need to use bias winding and associated external components.

Using a SOT-223 package, FSQ500L reduces total size and weight while increasing efficiency, productivity, and system reliability. Using FSQ500L, this design example for 2.04 W can be implemented with few external components and minimized cost.

1.2. Features

- Single-Chip 700 V SenseFET Power Switch
- Precision Fixed Operating Frequency: 130 kHz
- No-load consumption 250 mW at 265 V_{AC} with Burst Mode and Down to 60 mW with External Bias
- Internal Startup Switch
- Soft-Start Time Tuned by External Capacitor
- Under-Voltage Lockout (UVLO) with Hysteresis
- Pulse-by-Pulse Current Limit
- Overload Protection (OLP) and Internal Thermal Shutdown Function (TSD) with Hysteresis
- Auto-Restart Mode
- No Need for Auxiliary Bias Winding

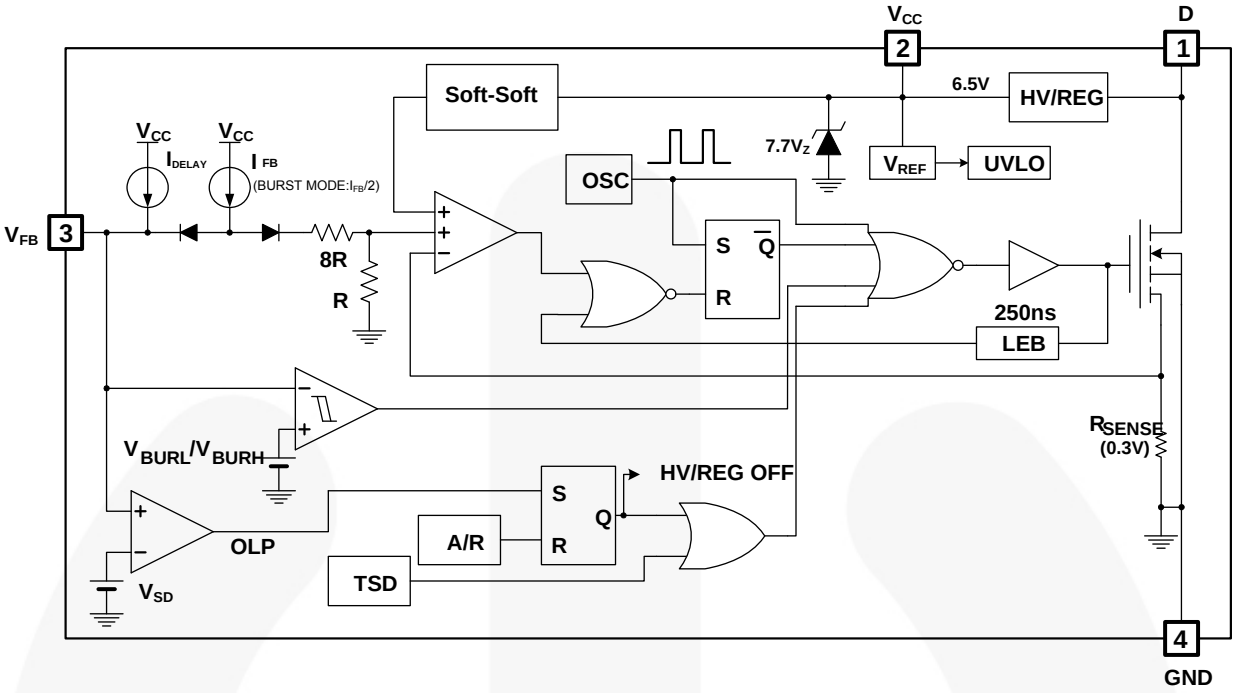


Figure 1. Internal Block Diagram

2. Specifications

Table 1. Summary of Features and Performance

Description	Min.	Max.	Unit
Input			
Voltage	90	264	V_{AC}
Frequency	47	63	Hz
Output			
Output Voltage 1		5.1	V
Output Current 1	0	0.4	A
Total Output Power			
Full-load Output Power	0	2.04	W
Peak Output Power			W

3. Photographs & PCB Layout

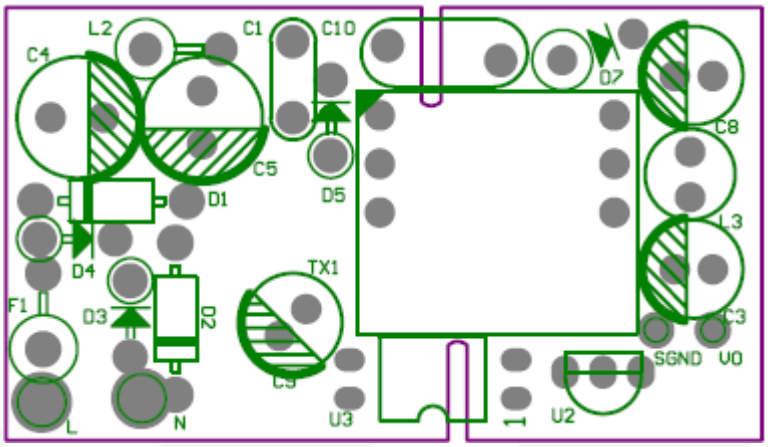


Figure 2. Top Overlay Silk Screen

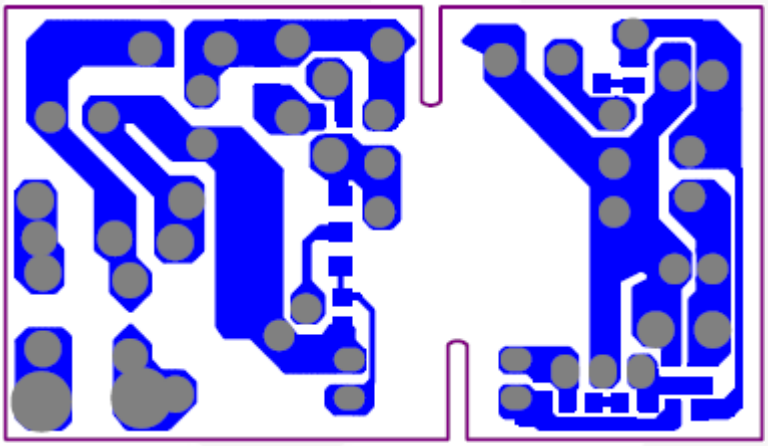


Figure 3. Bottom Layer Pattern

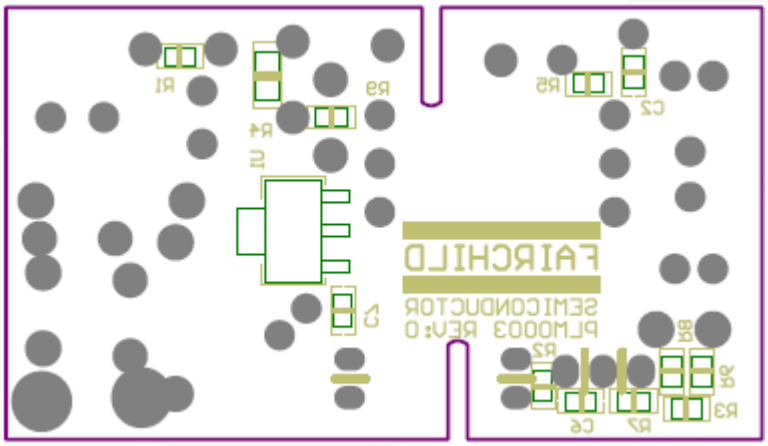


Figure 4. Bottom Overlay Silk Screen

4. Function Test Report

Test Model	FEBFSQ500L_H257v1
Test Date	June.23, 2008
Test Temperature	Ambient
Test Equipment	AC source: 6800 AC POWER SOURCE Electronic load: Chroma 63030 Power meter: WT210 Oscilloscope: LeCory 24Xs
Test Items	1 Input Current 2 Input Wattage at No-Load Condition 3 Burst Mode Test 4 Soft-Start Test 5 Turn-On Delay Test 6 DC Output Rising Time 7 Line and Load Regulation 8 Efficiency 9 Output Ripple and Noise 10 Step Load Response 11 Over-Current Protection 12 Hold-Up Time 13 Short Circuit Protection 14 Maximum Duty Ratio 15 Power Off 16 Over-Temperature Protection (OTP) 17 Voltage Stress of Drain and Secondary Rectifier 18 EMI Waveforms 19 Surge Test 20 ESD Test

4.1. Input Current

4.1.1. Test Condition

Measure the AC input current at maximum loading.

Table 2. Test Result

Input Voltage	Input Current
85 V_{AC} / 60 Hz	57.62 mA
264 V_{AC} / 50 Hz	35.73 mA

4.2. Input Wattage at No-Load Condition

4.2.1. Test Condition

Measure the input wattage and output voltage at no load.

Table 3. Test Result

Input Voltage	Input Wattage	Output Voltage	Specification
85 V_{AC} / 60 Hz	0.094 W	5.224 V	< 0.25 W
120 V_{AC} / 60 Hz	0.116 W	5.224 V	
230 V_{AC} / 50 Hz	0.209 W	5.224 V	
264 V_{AC} / 50 Hz	0.242 W	5.224 V	

4.3. Burst Mode Test

4.3.1. Test Condition

Measure the waveform and frequency in Burst Mode at no load.

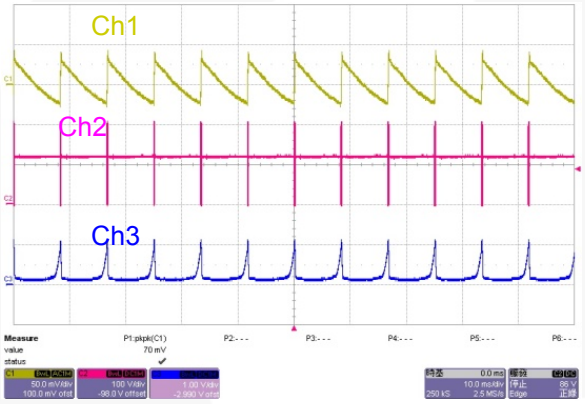


Figure 5. 85 V_{AC} / 60 Hz at No Load (Ch 1: Vo, Ch 2: V_{DS}, Ch 3: V_{FB})

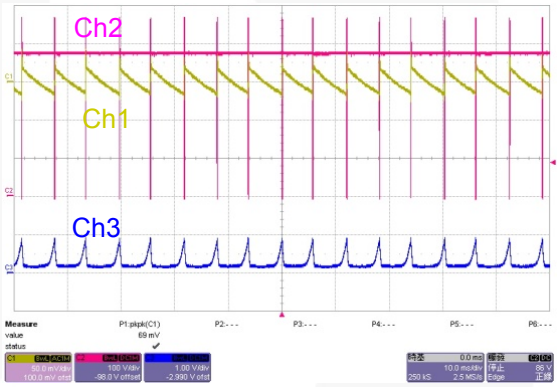


Figure 6. 264 V_{AC} / 50 Hz at No Load (Ch 1: Vo, Ch 2: V_{DS}, Ch 3: V_{FB})

4.4. Soft-Start Test

4.4.1. Test Condition

Measure the soft-start waveform at maximum load with ambient, after short, after OTP.

Table 4. Test Result

Input Voltage	Soft-Start Time
120 V_{AC} / 60 Hz	14 ms Under
240 V_{AC} / 50 Hz	14 ms Under

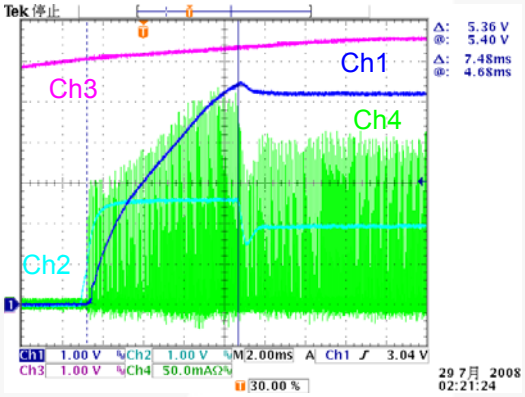


Figure 7. 120 V_{AC} / 60 Hz at Max. Load, Ambient (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

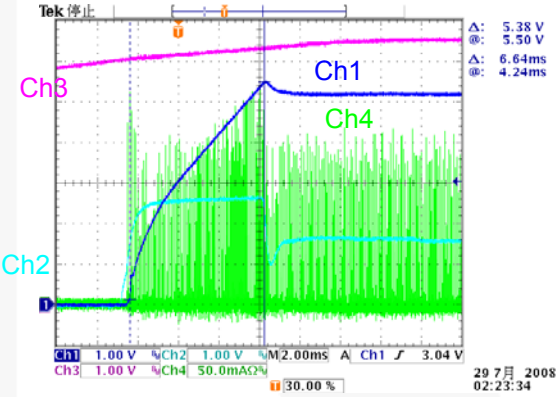


Figure 8. 240 V_{AC} / 50 Hz at Max. Load, Ambient (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

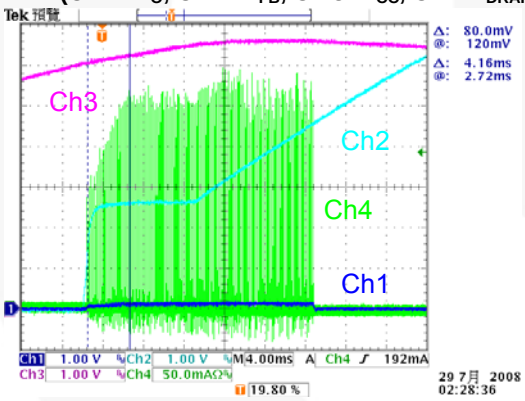


Figure 9. 120 V_{AC} / 60 Hz at Max. Load, After Short (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

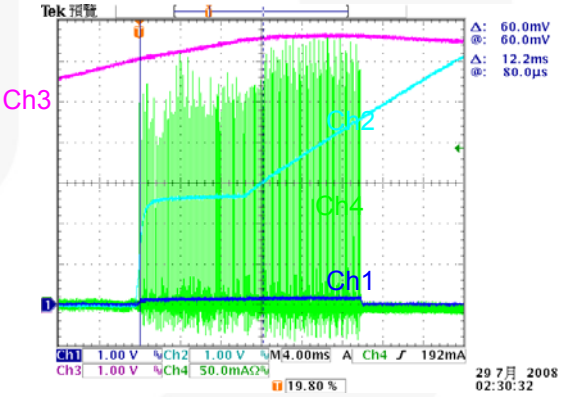


Figure 10. 240 V_{AC} / 50 Hz at Max. Load, After Short (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

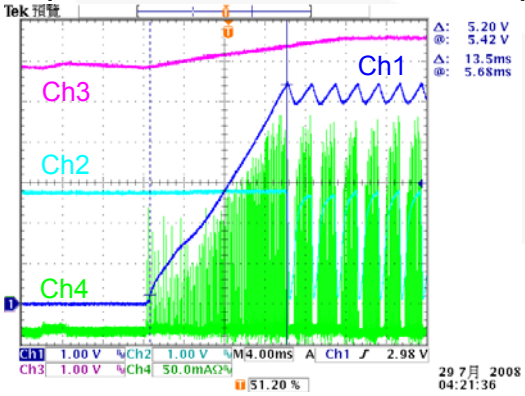


Figure 11. 120 V_{AC} / 60 Hz at Max. Load, After OTP (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

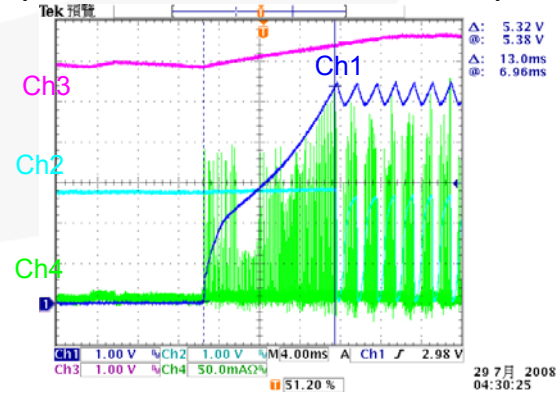


Figure 12. 240 V_{AC} / 50 Hz at Max. Load, After OTP (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

4.5. Turn-On Delay Test

4.5.1. Test Condition

Set the output at maximum loading. Measure the interval between AC plug-in and stable output.

Table 5. Test Result

Input Voltage	Maximum Load
85 V_{AC} / 60 Hz	89.60 ms
264 V_{AC} / 50 Hz	99.08 ms

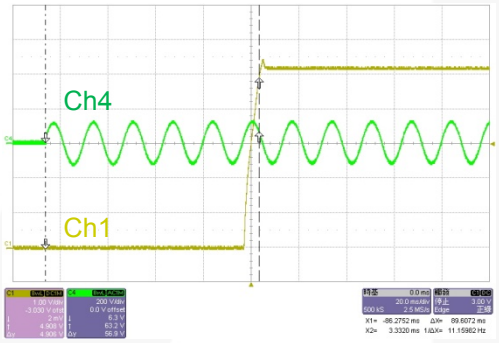


Figure 13. 85 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 4: V_{AC})

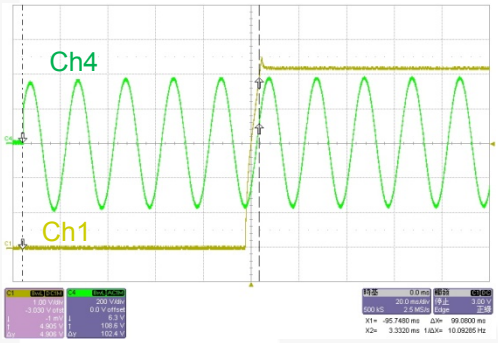


Figure 14. 264 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O, Ch 4: V_{AC})

4.6. DC Output Rising Time

4.6.1. Test Condition

Set output at maximum loading and no loading. Measure the time interval between 10% and 90% of output voltage during startup.

Table 6. Test Result

Input Voltage	Maximum Load	No Load	Specification
85 V_{AC} / 60 Hz	5.26 ms	4.04 ms	< 20 ms
264 V_{AC} / 50 Hz	5.05 ms	3.63 ms	

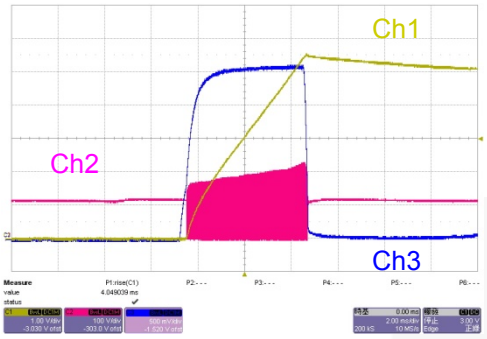


Figure 15. 85 V_{AC} / 60 Hz at No Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

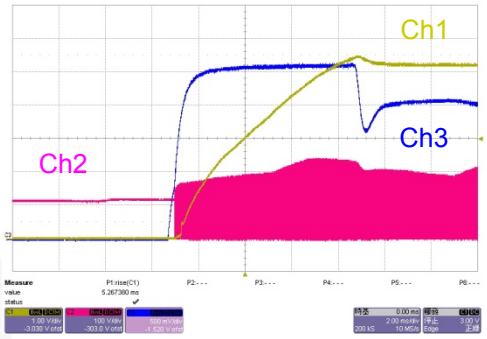


Figure 16. 85 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

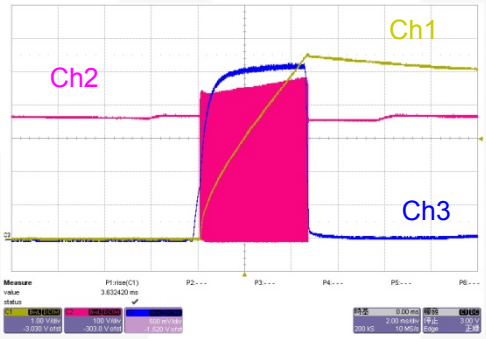


Figure 17. 264 V_{AC} / 50 Hz at No Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

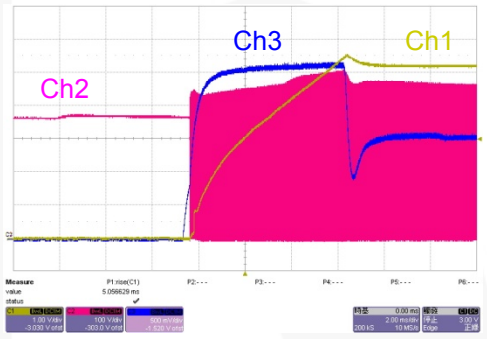


Figure 18. 264 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

4.7. Line and Load Regulation

4.7.1. Test Condition

Measure line and load regulation according to Table 7 (with output cable).

Table 7. Test Result

Input Voltage	Output Voltage at Max. Load	Output Voltage at Min. Load	Load Regulation
85 V_{AC} / 60 Hz	5.224 V	5.224 V	0%
115 V_{AC} / 60 Hz	5.224 V	5.224 V	0%
132 V_{AC} / 60 Hz	5.224 V	5.224 V	0%
180 V_{AC} / 50 Hz	5.224 V	5.224 V	0%
230 V_{AC} / 50 Hz	5.224 V	5.224 V	0%
264 V_{AC} / 50 Hz	5.224 V	5.224 V	0%
Line Regulation	0%	0%	

4.8. Efficiency

4.8.1. Test Condition

Output at maximum load.

Table 8. Test Result

Input Voltage	Input Wattage	Output Wattage	Efficiency
85 V_{AC} / 60 Hz	3.17 W	2.09 W	65.93%
120 V_{AC} / 60 Hz	3.15 W	2.09 W	66.34%
230 V_{AC} / 50 Hz	3.691 W	2.09 W	56.62%
264 V_{AC} / 50 Hz	3.933 W	2.09 W	53.14%

Table 9. Test Result

	Efficiency				
Input Voltage	**25% Load**	**50% Load**	**75% Load**	**100% Load**	**Average**
115 V_{AC} / 60 Hz	55.31%	58.88%	64.43%	66.22%	61.21%
230 V_{AC} / 50 Hz	43.01%	46.97%	50.96%	56.62%	49.41%

4.9. Output Ripple and Noise

4.9.1. Test Condition

Ripple and noise are measured by using a 20 MHz-bandwidth limited oscilloscope with a 10 µF capacitor paralleled with a high-frequency 0.1 µF capacitor across each output.

Table 10. Test Result

Input Voltage	Maximum Load	Minimum Load
85 V_{AC} / 60 Hz	16 mV	69 mV
120 V_{AC} / 60 Hz	19 mV	69 mV
240 V_{AC} / 50 Hz	16 mV	53 mV
264 V_{AC} / 50 Hz	16 mV	50 mV

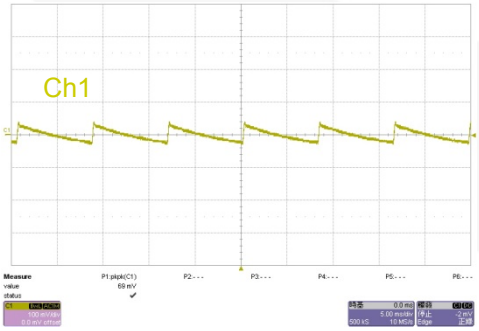


Figure 19. 85 V_{AC} / 60 Hz at No Load (Ch 1: V_O)

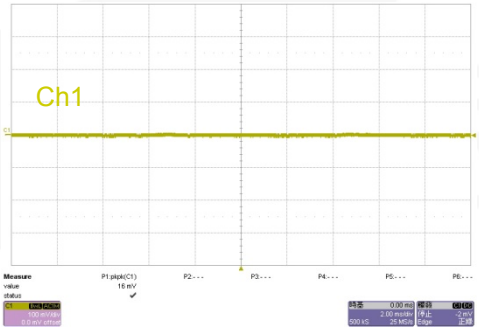


Figure 20. 85 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O)

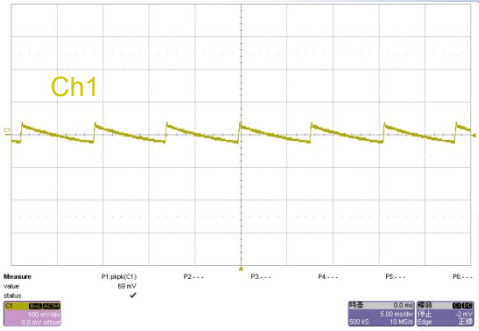


Figure 21. 120 V_{AC} / 60 Hz at No Load (Ch 1: V_O)

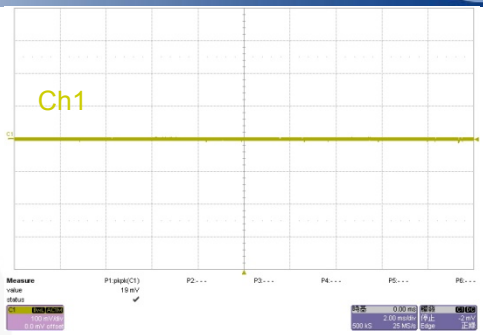


Figure 22. 120 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O)

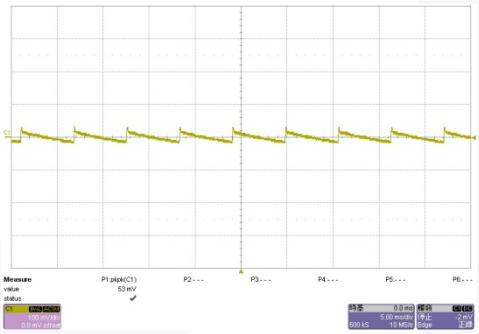


Figure 23. 24 0V_{AC} / 50 Hz at No Load (Ch 1: V_O)

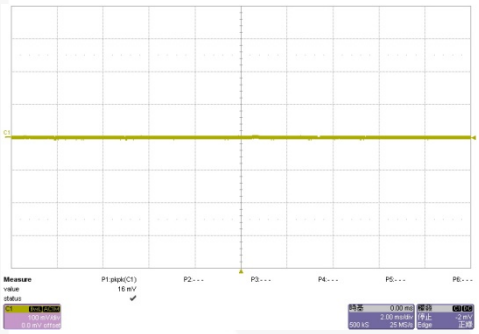


Figure 24. 240 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O)

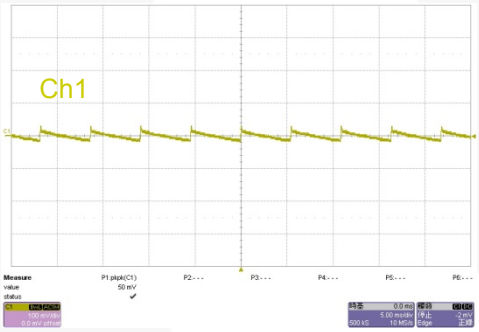


Figure 25. 264 V_{AC} / 50 Hz at No Load (Ch 1: V_O)

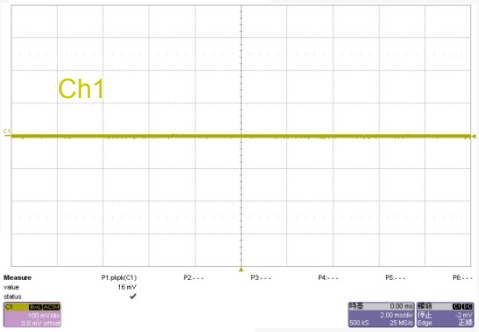


Figure 26. 264 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O)

4.10. Step Load Response

4.10.1. Test Condition

Dynamic loading (20%~80% of the full load, 5 ms duty cycle, 2.5 A/µs rise/fall time).

Table 11. Test Result (20%~80% of the Full Load)

Input Voltage	Overshoot	Undershoot
85 V_{AC} / 60 Hz	70 mV	53 mV
264 V_{AC} / 50 Hz	61 mV	119 mV

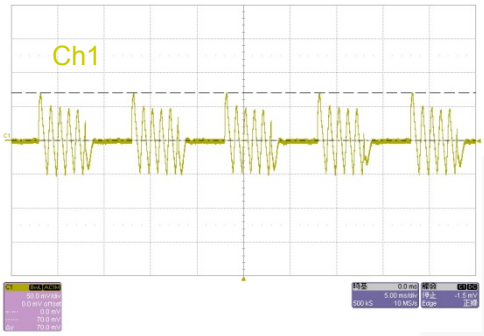


Figure 27. 85 V_{AC} / 60 Hz (Ch 1: V_O)

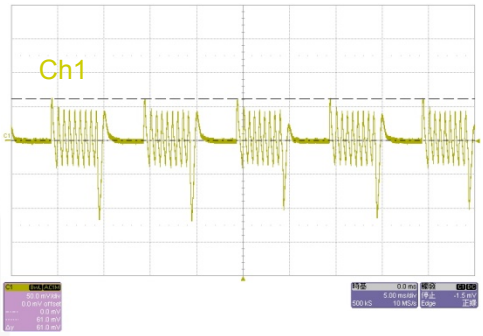


Figure 28. 264 V_{AC} / 50 Hz (Ch 1: V_O)

4.11. Over-Current Protection

4.11.1. Test Condition

Increase output loading gradually and measure the maximum output power.

Table 12. Test Result

Input Voltage	Output Current
85 V_{AC} / 60 Hz	0.611 A
120 V_{AC} / 60 Hz	0.650 A
240 V_{AC} / 50 Hz	0.836 A
264 V_{AC} / 50 Hz	0.881 A

4.12. Hold-up Time

4.12.1. Test Condition

Set output at maximum load. Measure the time interval between AC off and output voltage falling to the lower limit of the rated value. The AC waveform should be off at zero phase.

Table 13. Test Result

Input Voltage	Hold-up Time
85 V_{AC} / 60 Hz	8.49 ms
115 V_{AC} / 60 Hz	18.64 ms
230 V_{AC} / 50 Hz	77.27 ms
264 V_{AC} / 50 Hz	101.41 ms

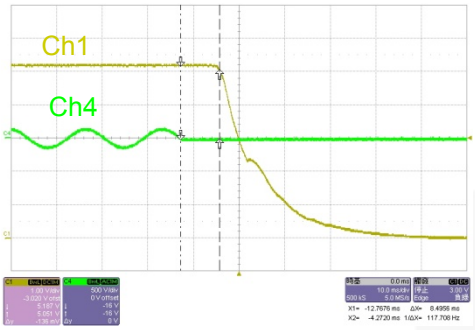


Figure 29. 85 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

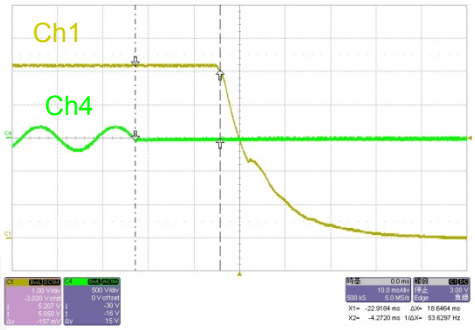


Figure 30. 115 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

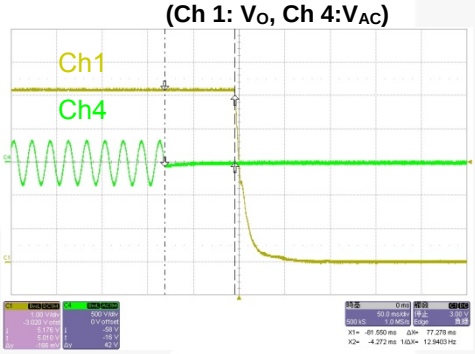


Figure 31. 230 V_{AC} / 50 Hz at No Load (Ch 1: V_O, Ch 4:V_{AC})

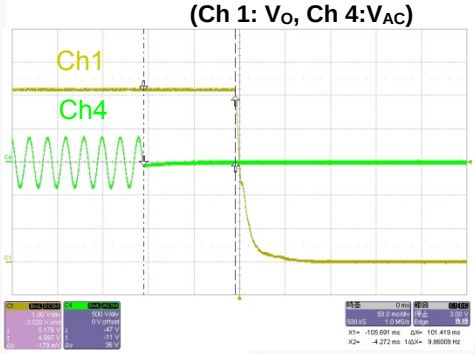


Figure 32. 264 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

4.13. Short Circuit Protection

4.13.1. Test Condition

Short the output of the power supply. The power supply should enter "Auto Restart Mode" protection with less than 2 W input voltage.

Table 14. Test Result

Input Voltage	Input Wattage at Maximum Load	Input Wattage at Minimum Load	Specification
120 V_{AC} / 60 Hz	0.574 W	0.572 W	Pin < 2 W
240 V_{AC} / 50 Hz	0.82 W	0.824 W	

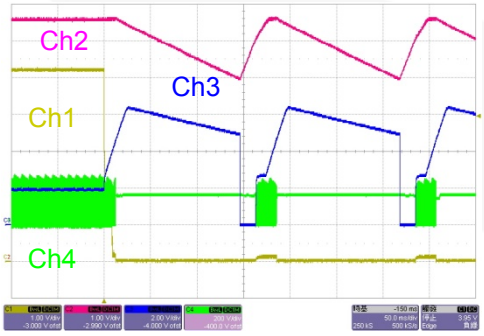


Figure 33. 120 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

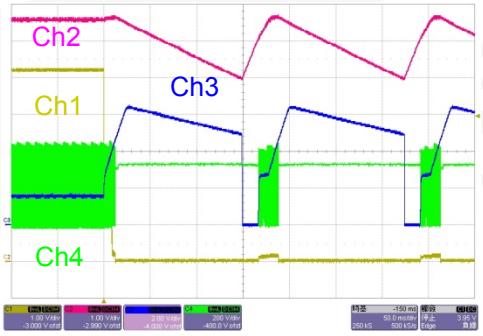


Figure 34. 240 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

4.14. Maximum Duty Ratio

4.14.1. Test Condition

Set the output at maximum loading. Decrease the input voltage with 5 V_{AC} step. Verify the FB voltage is under overload state (between 2.7~4 V). Measure the maximum duty and waveform.

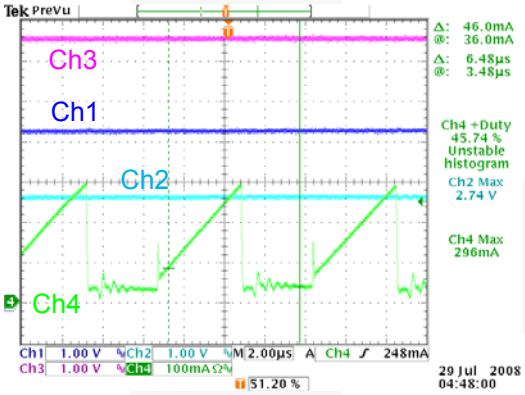


Figure 35. 50 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

4.15. Power Off

4.15.1. Test Condition

Set the output at the maximum load. Remove power.

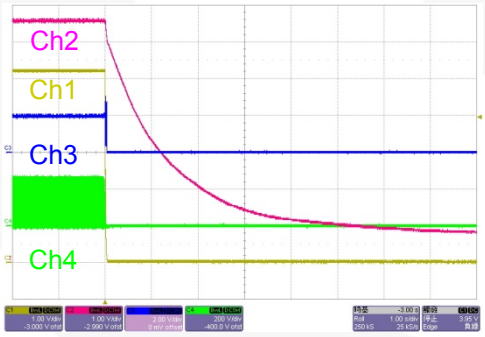


Figure 36. 120 V_{AC} / 60 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

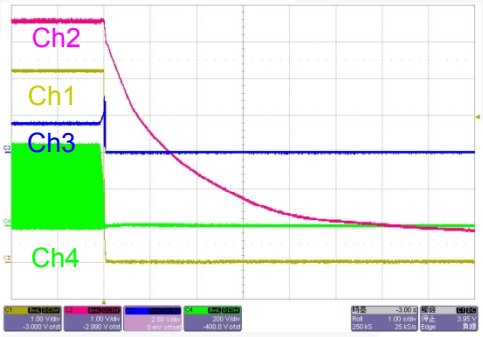


Figure 37. 240 V_{AC} / 50 Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

4.16. Over-Temperature Protection (OTP)

4.16.1. Test Condition

Set the output at maximum loading. Heat the IC with a heatgun, measure the waveform to enable the OTP, and disable the OTP.

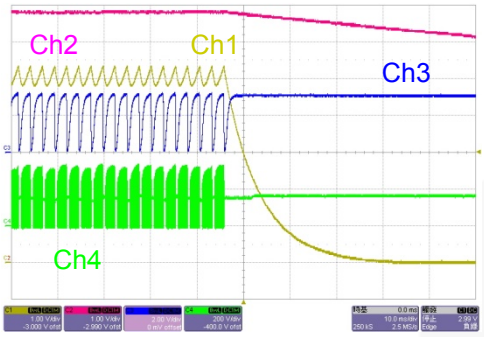


Figure 38. 120 V_{AC} / 60 Hz at Max. Load, Enable (Ch 1: V_O, Ch 2: V_{CC}. Ch 3: V_{FB}, Ch 4: V_{DS})

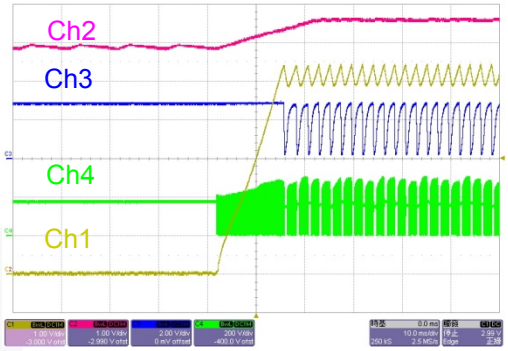


Figure 39. 120 V_{AC} / 60 Hz at Max. Load, Disable (Ch 1: V_O, Ch 2: V_{CC}. Ch 3: V_{FB}, Ch 4: V_{DS})

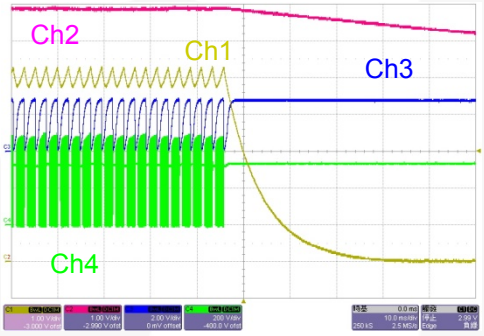


Figure 40. 240 V_{AC} / 50 Hz at Max. Load, Enable (Ch 1: V_O, Ch 2: V_{FB}. Ch 3: V_{CC}, Ch 4:V_{DS})

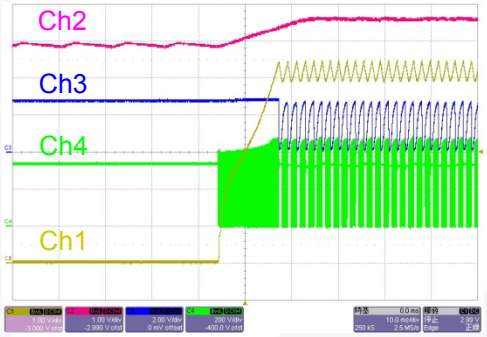


Figure 41. 240 V_{AC} / 50 Hz at Max.Load, Disable (Ch 1: V_O, Ch 2: V_{FB}. Ch 3: V_{CC}, Ch 4:V_{DS})

4.17. Voltage Stress of Drain and Secondary Rectifier

4.17.1. Test Condition

Measure the voltage stress of drain and secondary rectifiers under conditions specified in the table below.

4.17.2. Test Result

	Stress On MOSFET	Rating	Stress On Output Rectifier	Rating
85 V_{AC} / 60 Hz, Maximum Load	231 V	600 V	19.4 V	60 V
85 V_{AC} / 60 Hz, Maximum Load, Startup	234 V		18.8 V	
85 V_{AC} / 60 Hz, Maximum Load, Output Short	212 V		13.8 V	
264 V_{AC} / 50 Hz, Maximum Load	500 V		41.3 V	
264 V_{AC} / 50 Hz, Maximum Load, Startup	496 V		41.3 V	
264 V_{AC} / 50 Hz, Maximum Load, Output Short	471 V		35.6 V	
264 V_{AC} / 50 Hz, Maximum Load, Turns Off	494 V		41.3 V	

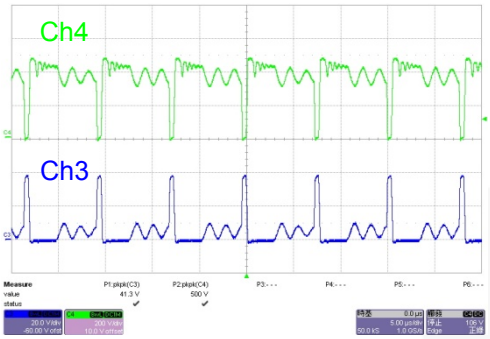


Figure 42. 264 V_{AC} / 50 Hz at Max. Load, Operating (Ch 3: $V_{ak\_rectifier}$, Ch 4:V_{DS_MOS})

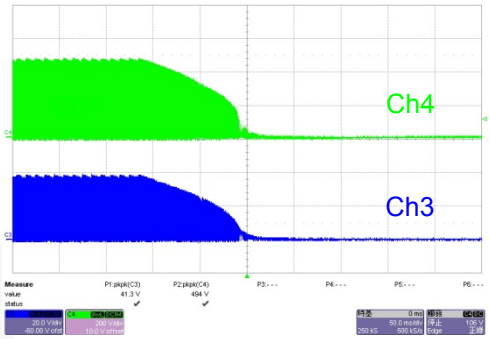


Figure 43. 264 V_{AC} / 50 Hz at Max. Load, Power Off (Ch 3: $V_{ak\_rectifier}$, Ch 4:V_{DS_MOS})

4.18. EMI Waveforms

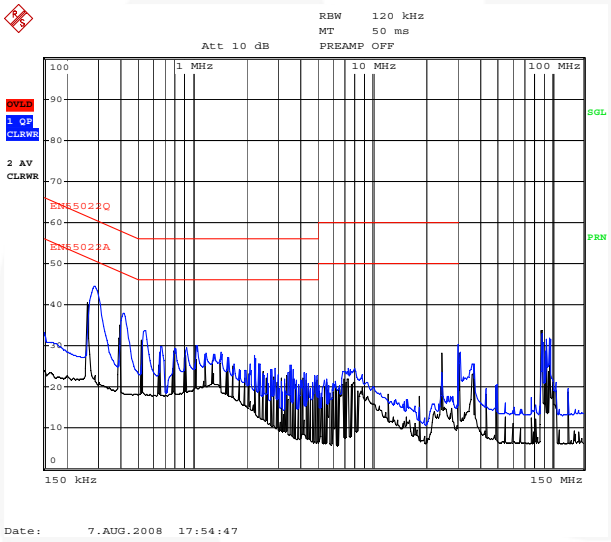


Figure 44. Conduction-Line at 115 V_{AC}

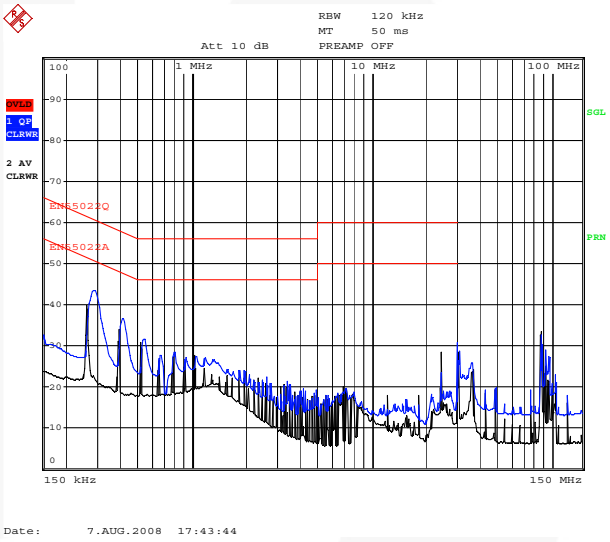


Figure 45. Conduction-Neutral at 115 V_{AC}

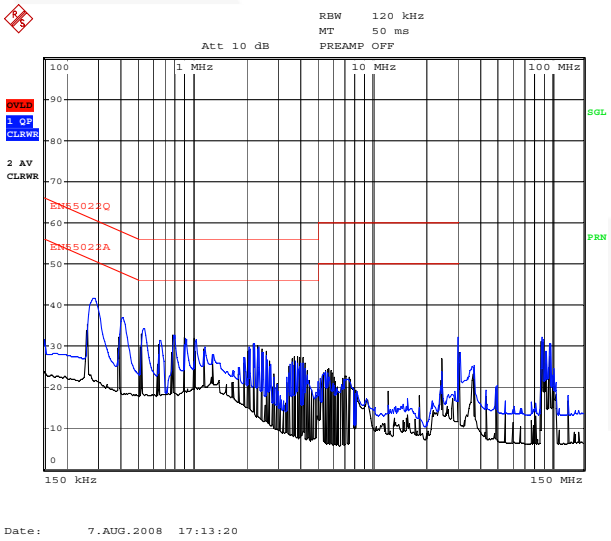


Figure 46. Conduction-Line at 230 V_{AC}

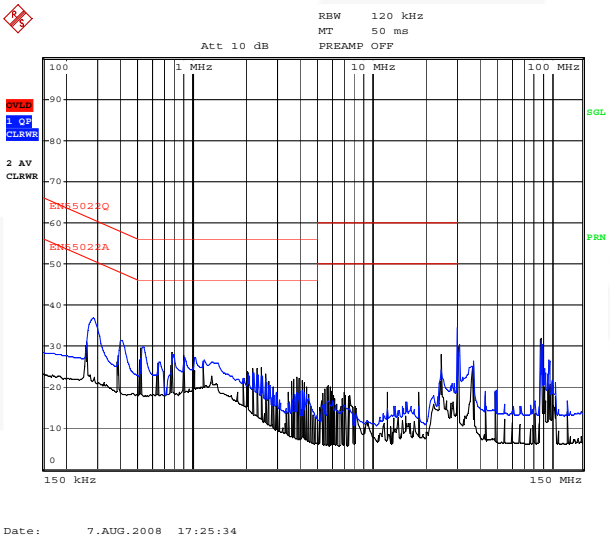


Figure 47. Conduction-Neutral at 230 V_{AC}

4.19. Surge Test

Mode	Polarity	Phase	Voltage	Condition
L-PE	±	0°	4.4 KV	Pass
	±	90°		Pass
	±	180°		Pass
	±	270°		Pass
N-PE	±	0°	4.4 KV	Pass
	±	90°		Pass
	±	180°		Pass
	±	270°		Pass

4.20. ESD Test

Air Discharge (16.5 KV)		Contact Discharge (8.8 KV)	
Pass	Pass	Pass	Pass

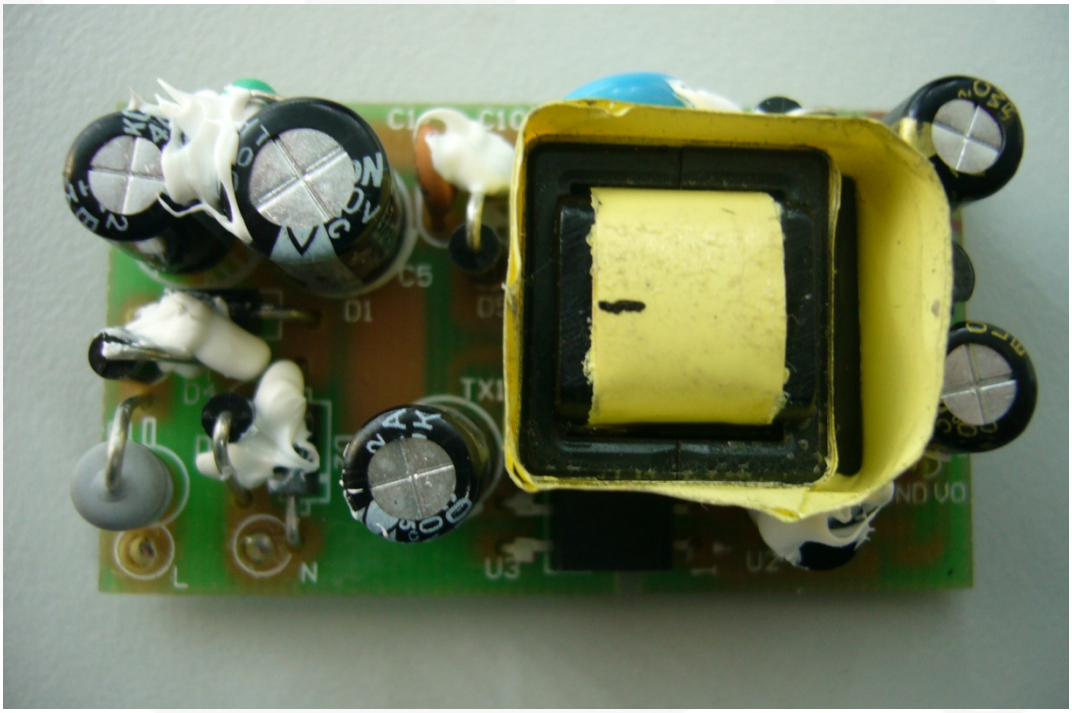


Figure 48. ESD Test Setup

5. Schematic

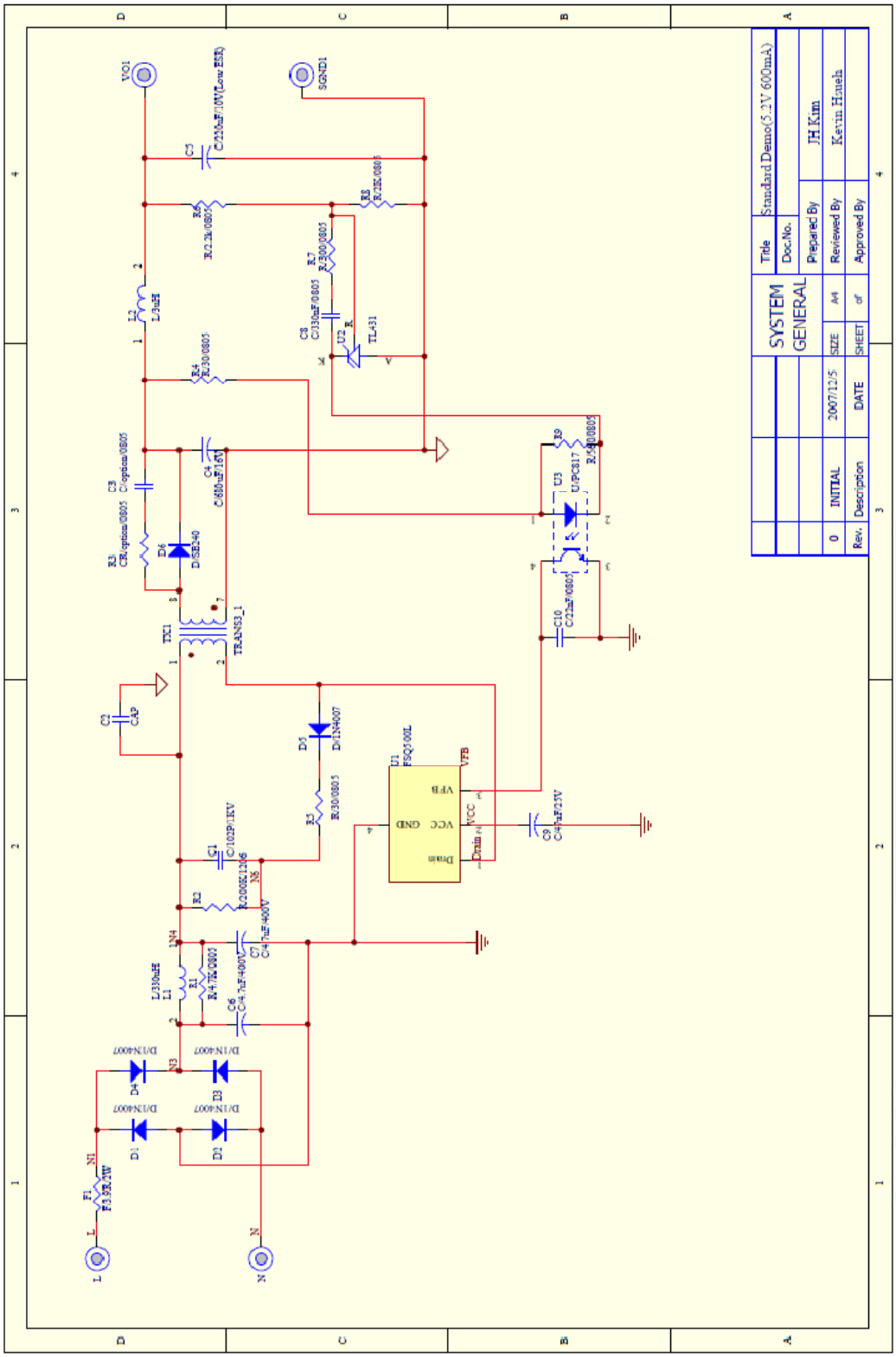
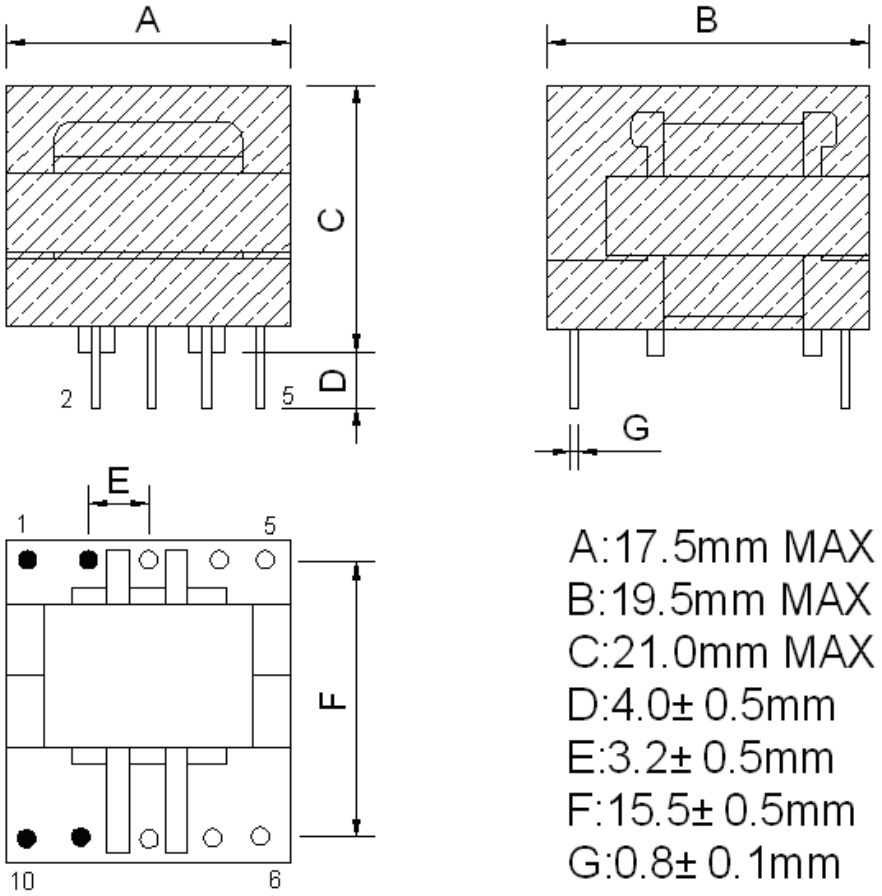


Figure 49. Schematic

6. Transformer Specification

Customer				P/N:	TRN-0246
DATE	08/12/2008	Version	A	Page	1/3

1.Dimension:



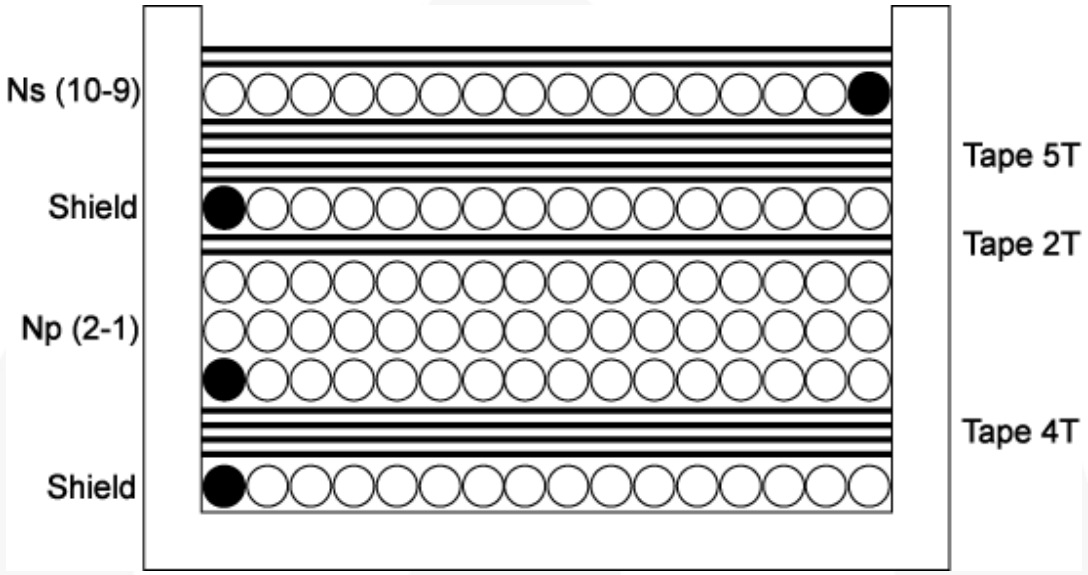
A:17.5mm MAX
B:19.5mm MAX
C:21.0mm MAX
D:4.0± 0.5mm
E:3.2± 0.5mm
F:15.5± 0.5mm
G:0.8± 0.1mm

Note:
1 .Pin3.4.5.6.7.8.removed

UNIT	m/m	DRAWN	CHECK	TITLE	TRANS
TEL	(02)2215-8302	Ci wun Chen	Guo long Huang	IDENT N O.	TRN-0246
FAX	(02)2215-8293	SEN HUEI INDUSTRIAL CO.,LTD.		D W G N O.	

Customer				P/N:	TRN-0246
DATE	08/12/2008	Version	A	Page	2/3

2.Schematic:



NO	TERMINAL		WIRE	T_S	INSUALTION	BARRIER	
	S	F			T_S		S
w1	1	x	0.15*1	46	4		
w2	2	1	0.2*1	104	2		
w3	1	x	0.15*1	46	5		
w4	10	9	TEX-E 0.4*1	9	2		
			CORE ROUNDING TAPE		3		

Customer				P/N:	TRN-0246
DATE	08/12/2008	Version	A	Page	3/3

3.Electrial Specification:

3.1 Inductance test： at 100 KHz ,1 V

P(2-1)： 800 μH ±5%

3.2 DC Resistance test at 25°C

P(2-1)：xx Ω Max. (not fixed)

P(10-9)：xx Ω Max. (not fixed)

3.3 Hi-pot test：

AC 3.0 KV /60 Hz/5 mA hi-pot for one minute between pri to sec.
AC 1.5 KV /60 Hz/5 mA hi-pot for one minute between pri to core.
AC 1.5 KV /60 Hz/5 mA hi-pot for one minute between sec to core.

3.4 Insulation test：

The insulation resistance is between pri to sec and windings to core measured by DC 500 V, must Be over 100 MΩ.

3.5 Terminal strength：

1.0 Kg on terminals for 30 seconds, test the breakdown.

UNIT	m/m	DRAWN	CHECK	TITLE	TRANS
TEL	(02)2215-8302	Ci wun Chen	Guo long Huang	IDENT N O.	TRN-0246
FAX	(02)2215-8293	SEN HUEI INDUSTRIAL CO.,LTD.		D W G N O.	
No.26-1, Lane 128, Sec. 2, Singnan Rd., Jhonghe City, Taipei County 235, Taiwan					

7. Bill of Materials

Item Number	Part Reference	Part Number	Quantity	Description (Manufacturer)
1	F1	TAPING	1	Metal-Oxide Resistor 1 W-S 10Ω ±5%
2	R3 R9	REEL	2	SMD Resistor 0805 30 Ω ±5%
3	R7	REEL	1	SMD Resistor 0805 300 Ω ±5%
4	R2	REEL	1	SMD Resistor 0805 1 KΩ ±1%
5	R8	REEL	1	SMD Resistor 0805 2 KΩ ±1%
6	R6	REEL	1	SMD Resistor 0805 2K2Ω ±1%
7	R1	REEL	1	SMD Resistor 0805 4K7Ω ±1%
8	R4	REEL	1	SMD Resistor 1206 200 KΩ ±5%
9	C5	8*11	1	Electrolytic Capacitor 4.7 µF 400 V 105°C
10	C9	6*11	1	Electrolytic Capacitor 47 µF 50 V 105°C
11	C4	6*11	1	Electrolytic Capacitor 1 µ 400 V 105°C
12	C8	6.3*11 LEK (Low ESR)	1	Electrolytic Capacitor 330 µF/10 V 105°C
13	C3	(Low ESR) ky10/220-L	1	Electrolytic Capacitor 220 µF/16 V 105°C
14	C1	Z5V	1	Ceramic Capacitor 102P 1 KV +80/-20%
15	C10	9.4*3.6	1	Y2 Capacitor 222P 250 V ±20%
16	C7	REEL	1	MLCC 0805 ±10% 223P 50 V
17	C6	REEL	1	MLCC 0805 ±10% 224P 50 V
18	L2	EC36-471K	1	Fixed Inductors 470 µH ±10%
19	L3	DR475C 15 µH	1	Inductor TRN0235
20	TX1	EE16,L=800 µH,4PIN	1	TRN0246 Transformer
21	D1, D2, D3, D4, D5	1N4007	5	Diode 1 A/1000 V DIP
22	D7	SB260	1	Schottky Diode 2 A/600 V DO-15
23	U1		1	SMD IC FSQ500L
24	U2	TO92	1	REGULATOR TL431ACZ-AP ±1% (Fairchild Semiconductor)
25	U3		1	IC PC817 DIP
26	PCS		1	PCB PLM-0003 REV0

8. Revision History

Rev.	Date	Description
1.0.0		Change User Guide EVB number from FEB257_001 to FEBFSQ500L_H257v1
1.0.1	3/6/12	Formatting & Editing pass by Tech Docs prior to posting
1.0.2	2/21/13	Change IC pin numbering on Figure 49