PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8733-01

700MHz Forward Error Correction Differential-to-3.3V LVPECL Clock Generator

General Description

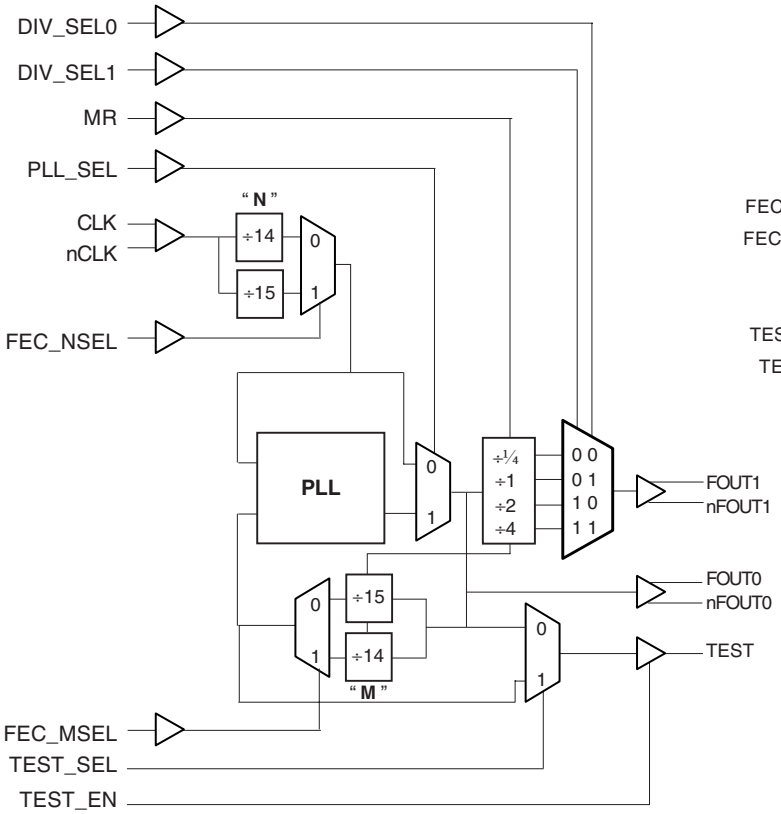
The ICS8733-01 is a dual output, Differential-to-3.3V LVPECL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8733-01 is designed to be used for applications utilizing Forward Error Correction (FEC) designs. The ICS8733-01 generates a 14/15 or a 15/14 output clock based upon the input reference clock in order to incorporate the FEC capability required by the application.

Clock generation is performed by a fully integrated and low-jitter phase-locked loop. The ICS8733-01 accepts any differential signal as its input with an input reference frequency range of 36.27MHz to 750MHz. There are two LVPECL outputs which can generate output frequencies of 38.88MHz to 700MHz.

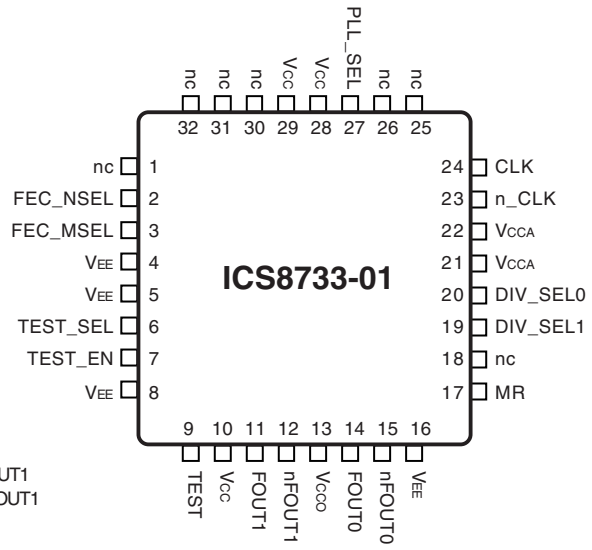
Features

- Clock synthesis of 14/15 or 15/14 of the input reference clock to be utilized in Forward Error Correction (FEC) applications
- Fully integrated PLL
- 2 differential 3.3V LVPECL outputs
- 1 differential clock input pair
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVHSTL, LVDS, SSTL, HCSL
- Output frequency range: 38.88MHz - 700MHz
- Input frequency range: 36.27MHz - 750MHz
- VCO range: 200MHz to 700MHz
- PLL bypass and test modes that support in-circuit testing and on-chip functional block characterization
- Cycle-to-cycle jitter: 20ps (typical)
- Period jitter: TBD
- Output skew: 10ps (maximum)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature

Block Diagram



Pin Assignment



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

Functional Description

The ICS8733-01 features a fully integrated PLL and therefore requires no external component for setting the loop bandwidth.

The ICS8733-01 will generate an output having a frequency as follows:

$$fREF\_CLK \times \frac{M}{N}$$

The M and N bits are controlled by the FEC_NSEL and FEC_MSEL control pins as shown in *Table 3A and Table 3B.*

As a result, FOUT0 can be configured to have an output frequency equal to 14/15, 15/14, 14/14, or 15/15 of the reference input frequency.

The second output clock (FOUT1) is configured to produce a frequency equal to FOUT0, FOUT/2, FOUT0/4, or FOUT0x4, dependent upon the DIV_SEL0 and DIV_SEL1 bits as shown in *Table 3C* and *3D.*

The reference input frequency range is dependent upon not only the M and N bits, but also upon the FOUT1 output configuration which is determined by the DIV_SEL0 and DIV_SEL1 bits. *Table 3C* shows the possible FOUT0 and FOUT1 output configurations as well as the reference input frequency range for each of these configurations.

The ICS8733-01 also supports in-circuit testing and on-chip functional block characterization via two test inputs and one test output. With the ICS8733-01 in PLL bypass mode (PLL_SEL = 0), the reference input bypasses the PLL and in-circuit testing of the N, M, and output dividers can take place. *Table 3D* shows the output configurations for the different combinations of the DIV_SEL1 and DIV_SEL0 pins.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 18, 25, 26, 30, 31, 32	nc	Unused		No connect.
2	FEC_NSEL	Input	Pulldown	Selects the N divide value. LVCMOS / LVTTL interface levels.
3	FEC_MSEL	Input	Pulldown	Selects the M divide value. LVCMOS / LVTTL interface levels.
4, 5, 8, 16	V_{EE}	Power		Negative supply pins. Connect to ground.
6	TEST_SEL	Input	Pulldown	Configures the TEST output pin to one of two different test modes. LVCMOS / LVTTL interface levels.
7	TEST_EN	Input	Pulldown	Enables the TEST output pin. LVCMOS / LVTTL interface levels.
9	TEST	Output		Output test pin. Programmed using TEST_SEL pin as shown in Table 3D.
10, 28, 29	V_{CC}	Power		Positive supply pins. Connect to 3.3V.
11, 12	FOUT1, nFOUT1	Output		Differential output for the generator. 3.3V LVPECL interface levels.
13	V_{CCO}	Power		Output supply pin. Connect to 3.3V.
14, 15	FOUT0, nFOUT0	Output		Differential ouput for the generator. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Resets the M, N, and output divider. Forces FOUT0 and FOUT1 low. LVCMOS / LVTTL interface levels.
19, 20	DIV_SEL1, DIV_SEL0	Input	Pulldown	Determines the output divide value for FOUT1. LVCMOS / LVTTL interface levels.
21, 22	V_{CCA}	Power		Analog supply pins. Connect to 3.3V.
23	nCLK	Input	Pullup	Inverting differential clock input.
24	CLK	Input	Pulldown	Non-inverting differential clock input.
27	PLL_SEL	Input	Pullup	Determines whether generator is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

Table 3A. FEC_NSEL Truth Table

FEC_NSEL	N
0	14
1	15

Table 3B. FEC-MSEL Truth Table

FEC_MSEL	M
0	15
1	14

Table 3C. Output Configuration and Input Frequency Range Table

Reference Input Frequency Range (MHz)									
DIV_SEL1	DIV_SEL0	FEC_NSEL	FEC_MSEL	Minimum Input Frequency (MHz)	Maximum Input Frequency (MHz)	Minimum FOUT0 (MHz)	Maximum FOUT0 (MHz)	Minimum FOUT1 (MHz)	Maximum FOUT1 (MHz)
0	0	0	0	36.27	81.67	38.86	87.50	155.44	350
0	0	0	1	36.27	87.5	36.27	87.50	145.08	350
0	0	1	0	38.88	87.5	38.88	87.50	155.52	350
0	0	1	1	38.88	93.75	36.29	87.50	145.15	350
0	1	0	0	93.3	326.67	100	350	100	350
0	1	0	1	100	350	100	350	100	350
0	1	1	0	100	350	100	350	100	350
0	1	1	1	107	375	100	350	100	350
1	0	0	0	186.7	653.33	200	700	100	350
1	0	0	1	200	700	200	700	100	350
1	0	1	0	200	700	200	700	100	350
1	0	1	1	214.3	750	200	700	100	350
1	1	0	0	186.7	653.33	200	700	50	175
1	1	0	1	200	700	200	700	50	175
1	1	1	0	200	700	200	700	50	175
1	1	1	1	214.3	750	200	700	50	175

Table 3D. Output Configuration Table and Test Mode Operation

DIV_SEL1	DIV_SEL0	PLL_SEL = 1		PLL_SEL = 0 and TEST_EN = 1			
		FOUT0	FOUT1	FOUT0	FOUT1	TEST TEST_SEL = 0	TEST TEST_SEL = 1
0	0	fREFxM/N	fREFx4M/N	fREF/4N	fREF/N	2fREF/N	fREF/2MN
0	1	fREFxM/N	fREFxM/N	fREF/N	fREF/N	2fREF/N	2fREF/MN
1	0	fREFxM/N	fREFx2M/N	fREF/N	fREF/2N	fREF/N	fREF/MN
1	1	fREFxM/N	fREFx4M/N	fREF/N	fREF/4N	fREF/N	fREF/MN

NOTE: In bypass mode, FOUT0 and FOUT1 will not always result in a 50% duty cycle.
Test output will never be 50% duty cycle.

Absolute Maximum Ratings

Supply Voltage, V_{CCx}	4.6V
Inputs, V_{CC}	-0.5V to V_{CC} + 0.5 V
Outputs, V_{CCO}	-0.5V to V_{CCO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current			TBD		mA
I_{CCA}	Analog Supply Current			TBD		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, DIV_SELx, PLL_SEL, MR		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, DIV_SELx, PLL_SEL, MR		-0.3		0.8	V
I_{IH}	Input High Current	FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, DIV_SELx, MR	$V_{CC} = V_{IN} = 3.465V$			150	µA
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	FEC_NSEL, FEC_MSEL, TEST_SEL, TEST_EN, DIV_SELx, MR	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	TEST; NOTE 1		2.6			V
V_{OL}	Output Low Voltage	TEST; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}/2$. See page 7, Figure 1, 3.3V Output Load Test Circuit.

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nCLK	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nCLK	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} + 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} -1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		0.85	V

NOTE 1: Outputs terminated with 50 Ω to V_{CCO} - 2V.

Table 5. Input Frequency Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		36.27		750	MHz

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{OUT}	Output Frequency		38.88		700	MHz
*t*jit(cc)	Cycle-to-Cycle Jitter, RMS; NOTE 1, 3			20		ps
*t*jit(per)	Period Jitter, RMS; NOTE 1, 3				TBD	ps
*t*sk(o)	Output Skew; NOTE 2, 3				10	ps
t_R	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle			50		%
t_{LOCK}	PLL Lock Time				10	ms

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

Parameter Measurement Information

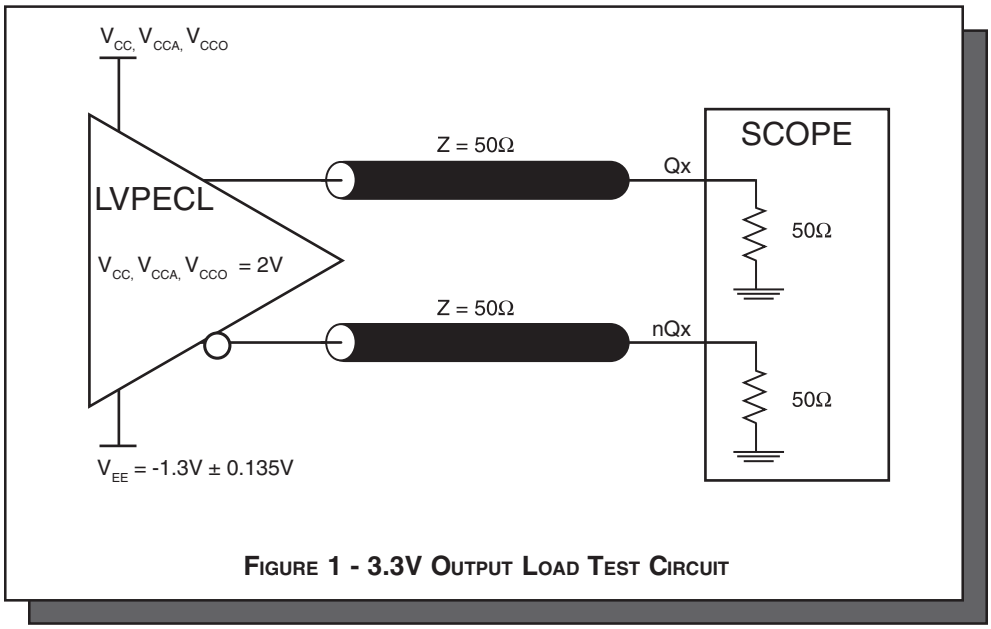


Figure 1 - 3.3V Output Load Test Circuit

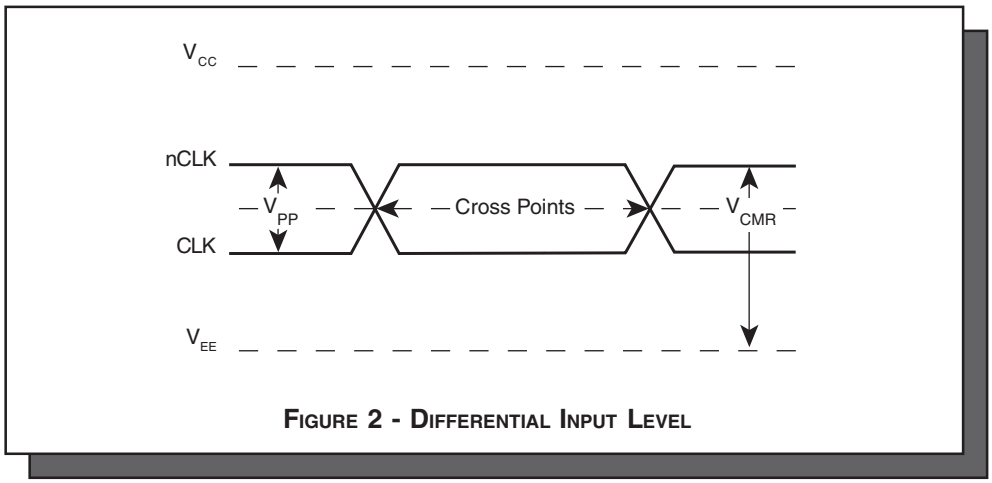


Figure 2 - Differential Input Level

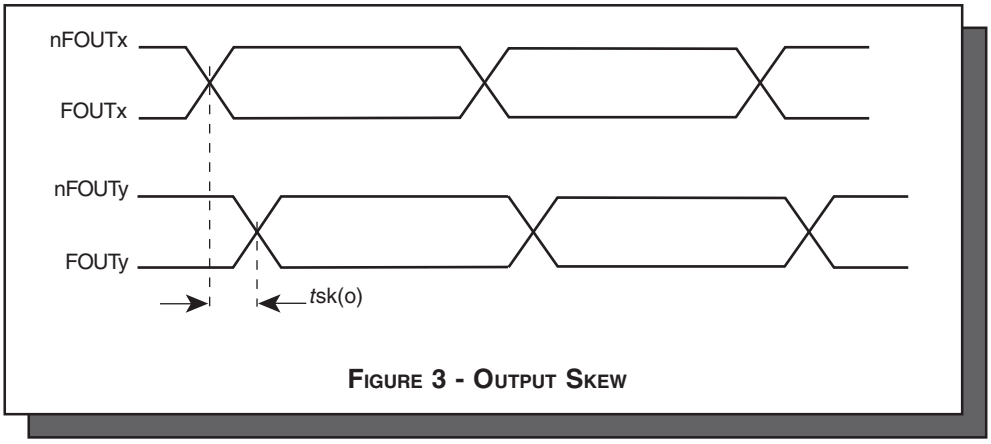
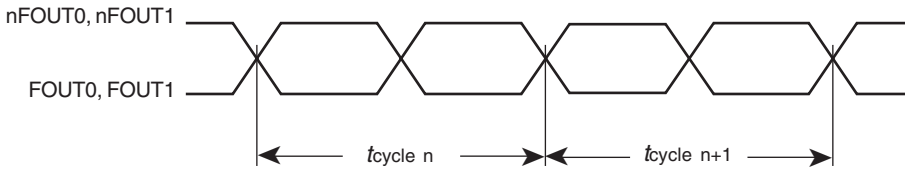


Figure 3 - Output Skew



$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

Figure 4 - Cycle-to-Cycle Jitter

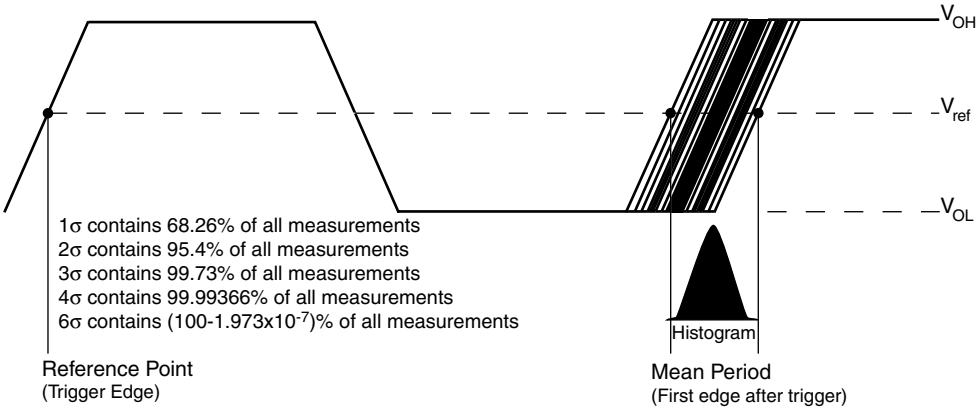


Figure 5 - Period Jitter

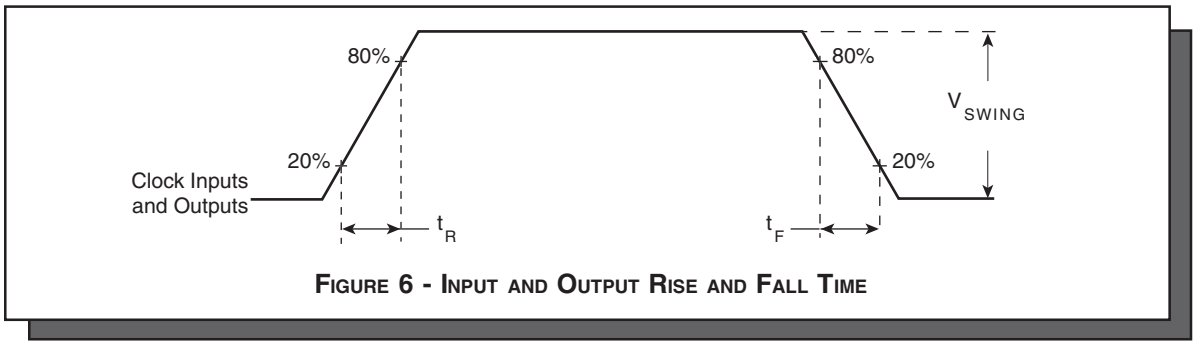


Figure 6 - Input and Output Rise and Fall Time

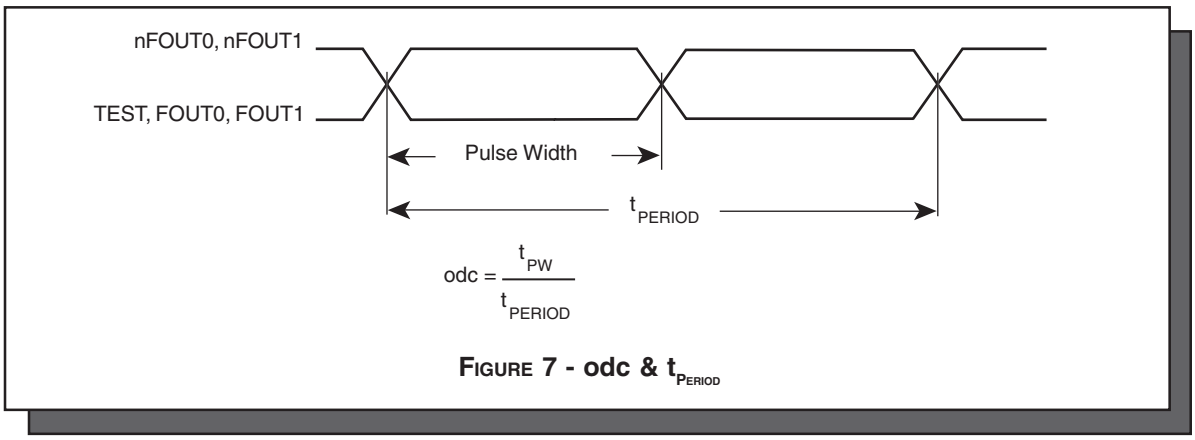


Figure 7 - odc & t_{PERIOD}

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

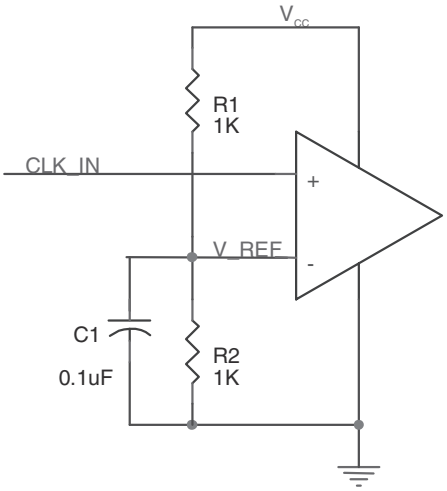


Figure 8 - Single Ended Signal Driving Differential Input

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8733-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 9* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

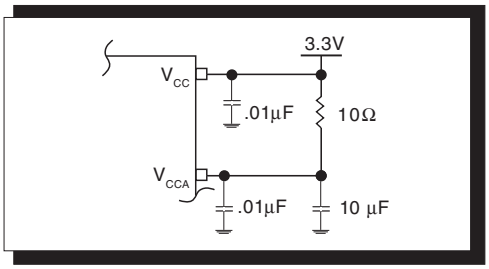


Figure 9 - Power Supply Filtering

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. There are a few simple termination schemes. *Figures 10A and 10B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

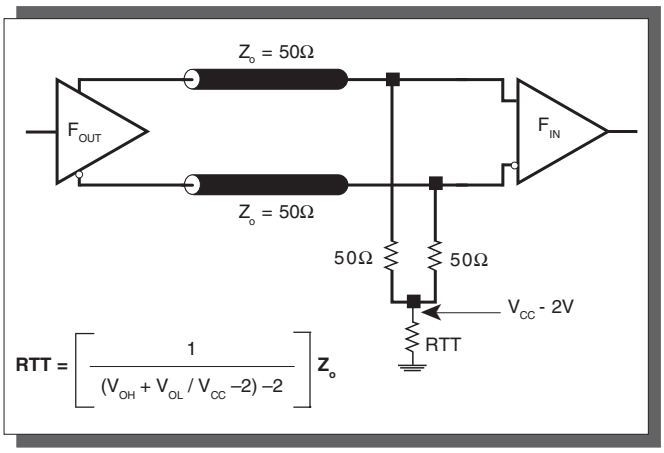


Figure 10A - LVPECL Output Termination

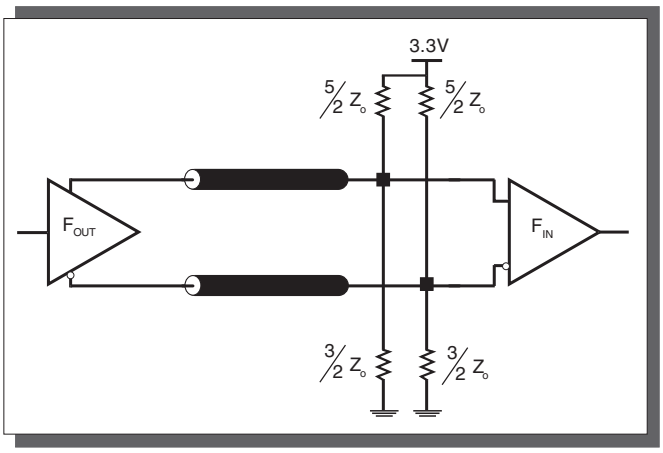


Figure 10B - LVPECL Output Termination

Layout Guideline

The schematic of the ICS8733-01 layout example used in this layout guideline is shown in *Figure 11A.* The ICS8733-01 recommended PCB board layout for this example is shown in *Figure 11B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stacking of the P.C. board.

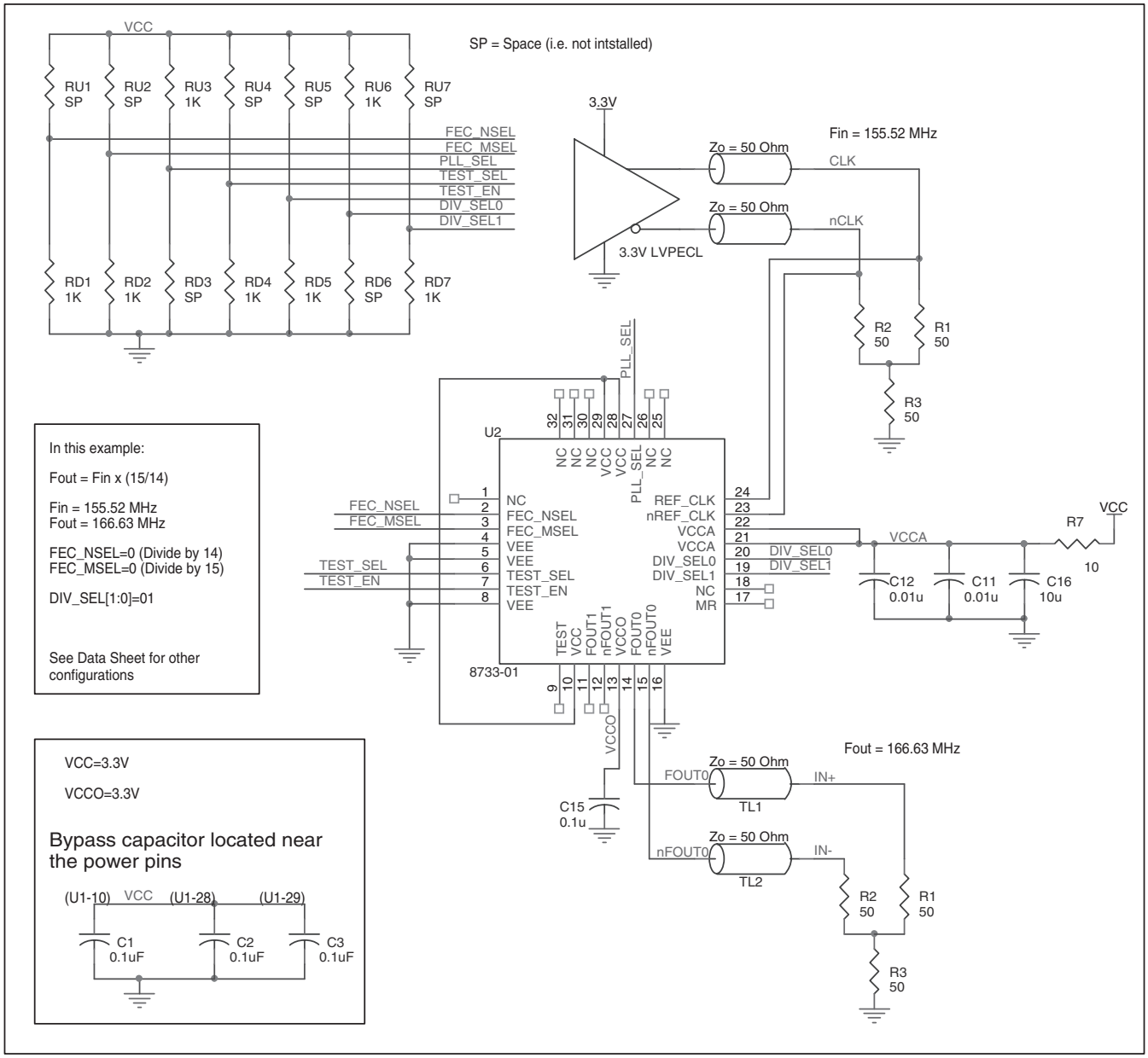


Figure 11A - Schematic of Recommended Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C2, C3, and C15, as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C16, C11, and C12 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a spearation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

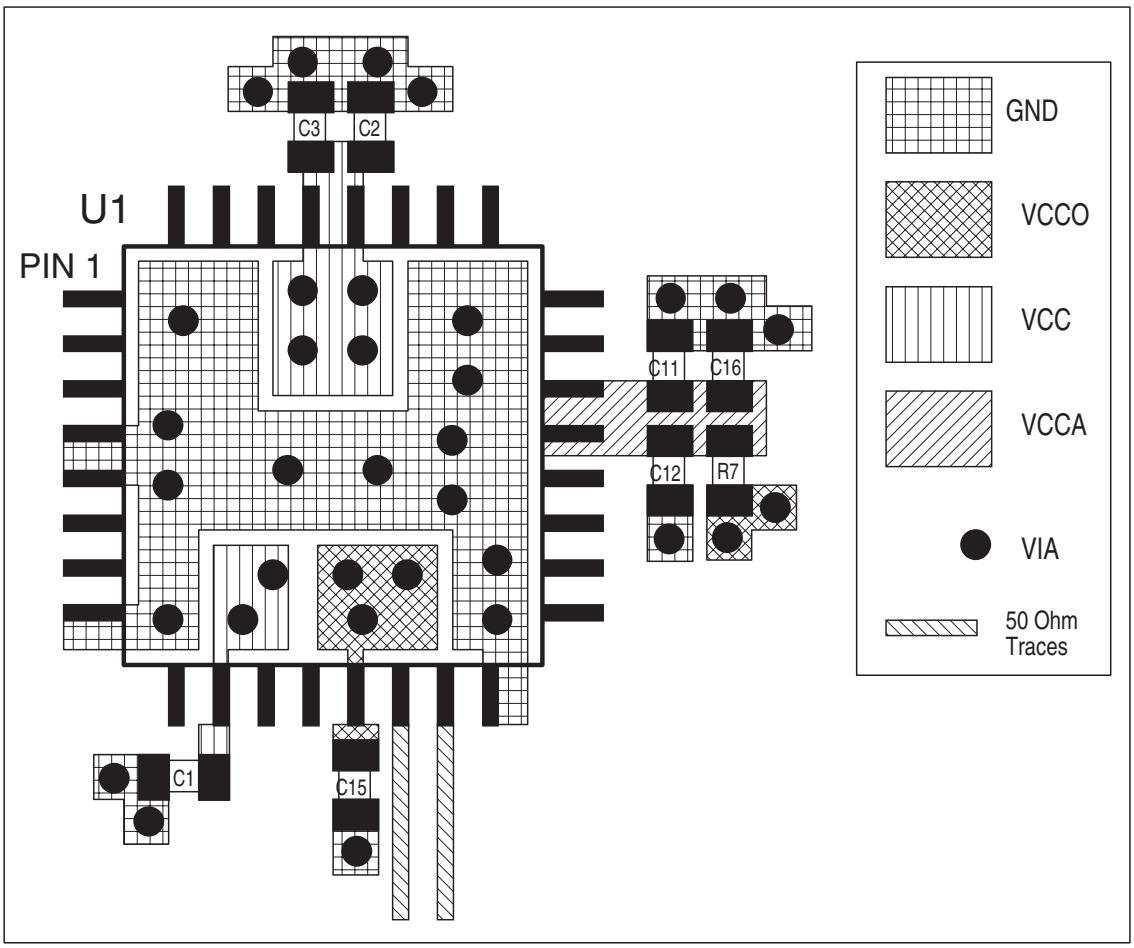


Figure 11B - PCB Board Layout for ICS8733-01

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8733-01.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8733-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 110mA = **381.2mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.2mW = **60.4mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 381.2mW + 60.4mW = **441.6mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.441W * 42.1°C/W = 88.6°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-pin LQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 12.*

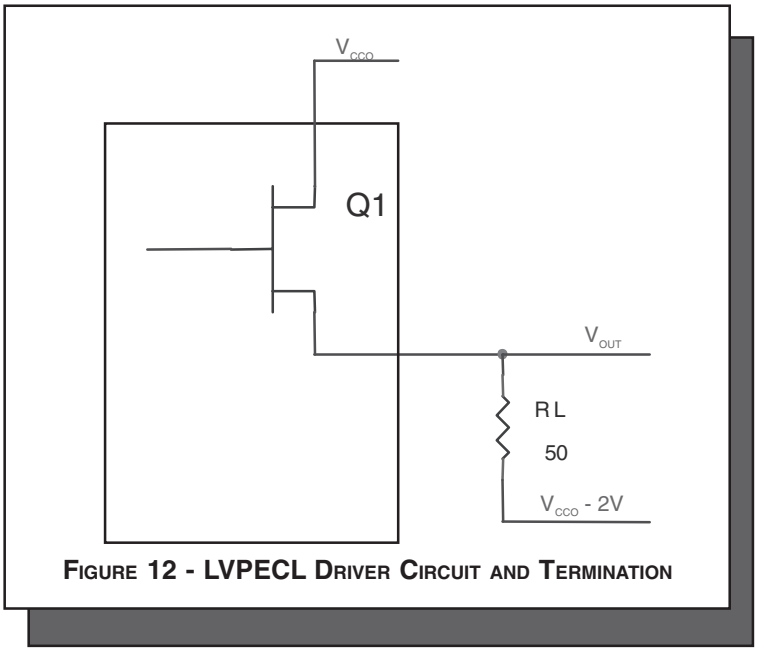


Figure 12 - LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS733-01 is: 3210

Package Outline - Y Suffix

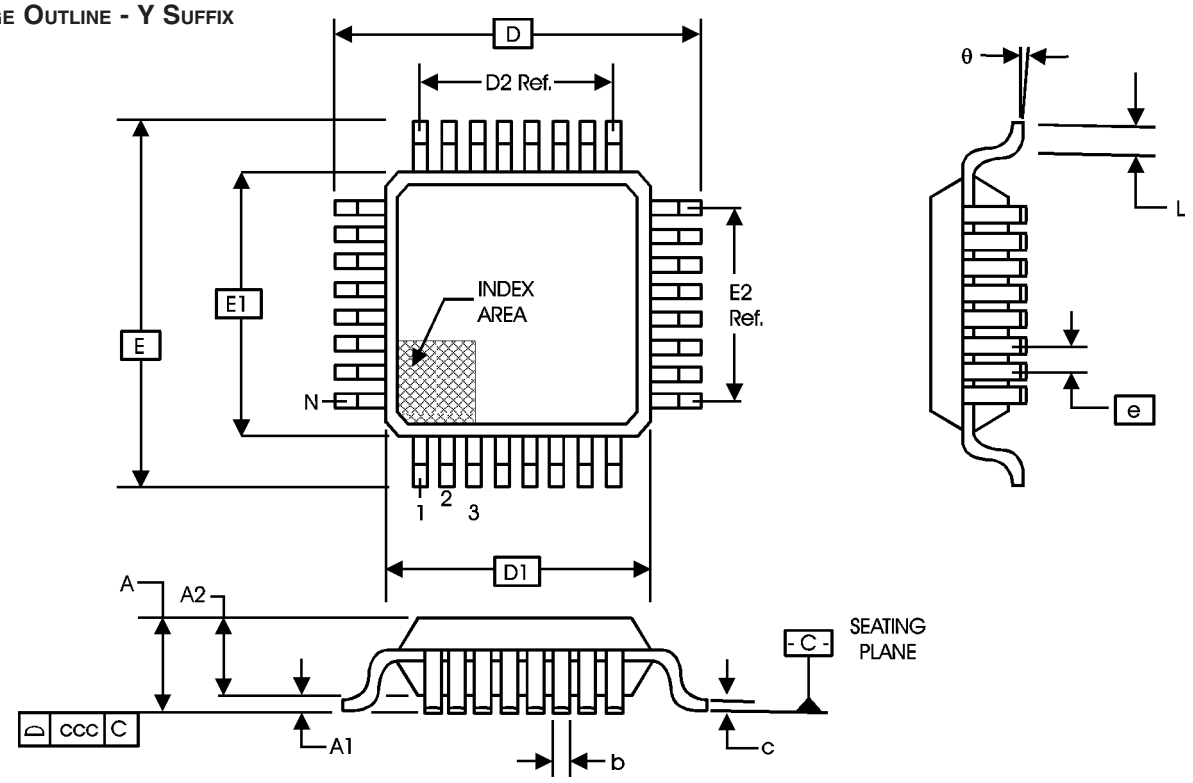


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

Table 10. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8733BY-01	ICS8733BY-01	32 Lead LQFP	250 per tray	0°C to 70°C
ICS8733BY-01T	ICS8733BY-01	32 Lead LQFP on Tape and Reel	1000	0°C to 70°C